

# First International Computer, Inc

## Portable Computer Group HW Department

Board name : MotherBoard Schematic

Project : **MR056B**

Version : 0.1

Initial Date : May. 04 , 2007

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LAN Circuit check by:

Audio Circuit check by:

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<b>Confidential</b>			
<b>MR056B</b>			
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# 1. Schematic Page Description :

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| 20. ICH8M PCI/PCIE/DMI(1/4)   | 40. MDC CNN                 |                                     |

## 2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD17	Mini PCI (Wireless LAN)
AD27	X
AD29	Lan (Realtek RTL8101L)


REQ	CHIP
REQ0 / GNT0	X
REQ1 / GNT1	LAN (Realtek RTL8101L)
REQ2 / GNT2	X
REQ3 / GNT3	X
REQ4 / GNT4	X

IRQ Channel	Description
IRQ0	System timer
IRQ1	Keyboard
IRQ2	(Casacde)
IRQ3	LAN / MODEM
IRQ4	<del>Serial Port</del>
IRQ5	AUDIO / VGA / USB
IRQ6	<del>FLOPPY DISK</del>
IRQ7	<del>LPT</del>
IRQ8	RTC
IRQ9	ACPI
IRQ10	FIR (Disable by default) (MODEM/LAN)
IRQ11	<del>Cardbus</del>
IRQ12	PS/2 mouse
IRQ13	FPU
IRQ14	HDD
IRQ15	CDROM

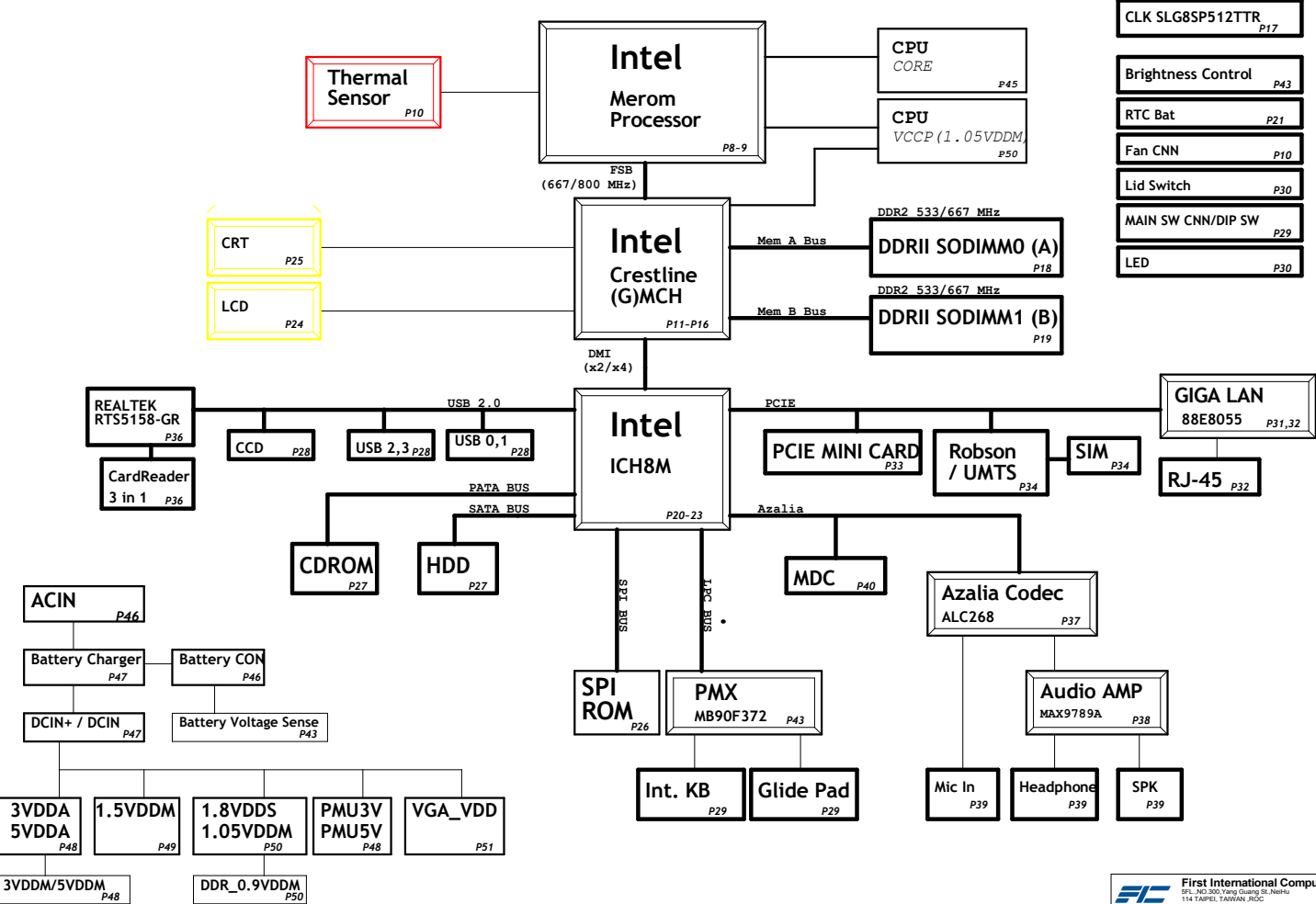
DMA Channel	Device
DMA0	FIR (disable by default) (MODEM / LAN)
DMA1	<del>EGP</del>
DMA2	<del>FLOPPY DISK</del>
DMA3	AUDIO
DMA4	(Cascade)
DMA5	Unused
DMA6	Unused
DMA7	Unused

PCIINT	CHIP
IRQA	IEEE1394 (VIA VT6311S)
IRQB	LAN (Realtek RTL8101L)
IRQC	X
IRQD	X
IRQE / GPIO2	LAN (Realtek RTL8101L)
IRQE / GPIO3	X
IRQE / GPIO4	PASS0
IRQE / GPIO5	CRISIS

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3. Block Diagram :



4. Nat name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON
3VDDA	3.3V always on power rail by DCON
3VDDS	3.3V power rail by PSUSC#
5VDDS	5.0V power rail by PSUSC#
3VDDM	3.3V switched power rail by SUSTAT_B#
5VDDM	5.0V switched power rail by SUSTAT_B#
VCC_CORE	Core Voltage for CPU
1.05VDDM	1.05V power rail for AGTL+ termination/Core for GMCH by SUSTAT_B#
1.5VDDM	1.5V power rail for CPU PLL/DMI/PCIE;DDRII DLLs for GMCH/Core;PCIE for ICH7m by SUSTAT_B#
1.8VDDS	1.8V power rail for DDRII by PSUSC#
0.9VDDT_DDRII	0.9V DDRII Termination Voltage by SUSTAT_B#

Part Naming Conventions

C	= Capacitor
CN	= Connector
D	= Diode
F	= Fuse
L	= Inductor
Q	= Transistor
R	= Resistor
RP	= Resistor Pack
U	= Arbitrary Logic Device
Y	= Crystal and Osc

Net Name Suffix


#	= Active Low signal
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5. Board Stack up Description

PCB Layers

Layer 1		Component Side, Microstrip signal Layer
Layer 2		Ground Plane
Layer 3		Stripline Layer(High Speed)
Layer 4		Stripline Layer(High Speed)
Layer 5		Power Plane
Layer 6		Solder Side, Microstrip signal Layer

	Single End Impedance	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SRC Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
Host Bus	55 ohm +/- 15%		
DDR2 CLK	42 ohm +/- 15%	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	55 ohm +/- 15%		85 ohm +/- 20%
DDR2 Bus	55 ohm +/- 15%		
DMI Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
PCIE Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SATA		95 ohm +/- 15%	100 ohm +/- 15%
SDVO	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
LVDS		100 ohm +/- 15%	100 ohm +/- 15%
USB		90 ohm +/- 15%	90 ohm +/- 15%
IEEE1394		110 ohm +/- 15%	110 ohm +/- 15%
Lan	50 ohm +/- 15%		

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~~Need Modify~~

Power Rail	Ball Name	Destination	Voltage	SO Current
2.5VDDM		945GM: PCIE analog 945GM: LVDS analog 945GM: LVDS I/O 945GM: CRT DAC CH7307:	2.32V~2.5V-2.625V 2.375V-2.5V-2.625V 2.375V-2.5V-2.625V 2.32V~2.5V-2.625V	2mA 10mA 60mA 70mA
3VDDM	VCCA_PEG_BG VCC_HV VCC_SYNC VCCA_CRT_DAC VCCA_TVA_DAC VCCA_TVB_DAC VCCA_TVC_DAC VCCA_DAC_BG	Crestline: PCI Express BaseGraphics Crestline: HV buffer power Crestline: H/VSNC power Crestline: CRT DAC Crestline: TV Out Crestline: TV Out Crestline: TV Out Crestline: TV DAC  ICH7m: Mini Card: Express Card: CLK Generator: ICS954226 KBC: KB3886 Flash ROM: BIOS Azalia Codec: ALC260 Azalia MDC: HDD: SATA	3.135V~3.3V~3.465V 3.135V~3.3V~3.465V    3.135V~3.3V~3.465V  3.0V~3.3V~3.6V	40mA 120mA       400mA
3VDD5		Lan: Broadcom BCM4401 Card Reader: SD/MMG/MS Azalia MDC: For wake up	3.0V~3.3V~3.6V	
3VDDA		ICH7m: ICH7m: ICH7m: LCD:	3.0V~3.3V~3.6V	1.0A
5VDDM		Azalia Codec: ALC260 Azalia MDC: HDD: SATA ODD: PATA Audio AMP: G1420 Inverter:	3.0V~3.3V~3.6V  4.75V~5.0V~5.25V 4.75V~5.0V~5.25V	Max: 1.0A ; R/W Max: 1.8A ; R/W: 900mA
5VDD5		USB: x 4 ports	5V	2.0A
PMU3V		EC: PMU08 ICH7m: RTC		

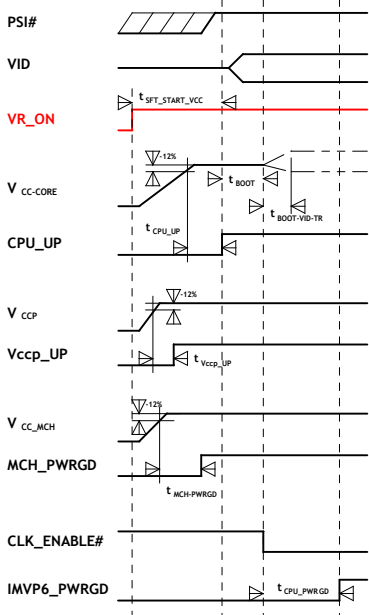
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Page22 RF_ON# change to RF_ON
Page22 UMTS_ON change to UMTS_OFF#
Page43 VOR0 change to VOR#

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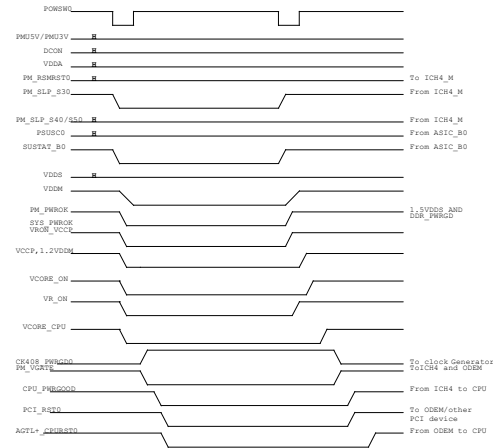
7. power on & off & S3 Sequence :

Power On Sequencing Timing Diagram  
20060117A - DATA FROM NO.16809

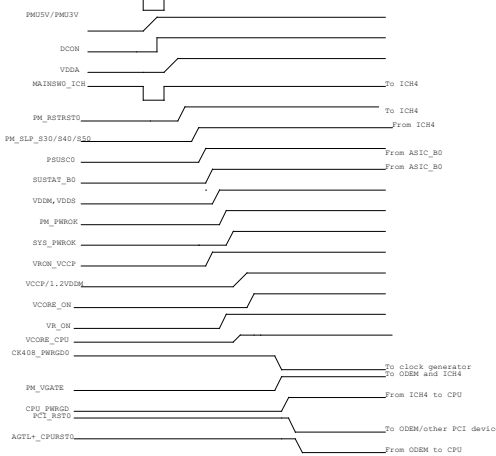


t <sub>SFT_START_VCC</sub>	Max = 3 ms
t <sub>BOOT</sub>	Min = 10 us , Max = 100 us
t <sub>BOOT-VID-TR</sub>	Max = 100 us
t <sub>CPU_UP</sub>	Min = 10 us , Max = 30 us
t <sub>VCCP_UP</sub>	Min = 10 us , Max = 30 us
t <sub>MCH-PWRGD</sub>	Min = 10 us , Max = 30 us
t <sub>CPU_PWRGD</sub>	Min = 3 ms , Max = 20 ms

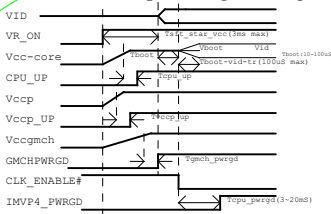
S3 SUSPEND AND RESUME TIMING



BATTERY ONLY POWER ON TIMING



IMVP6 Power On Sequencing Timing Diagram



8. Layout Guideline :

Crestline DDRII Layout Guidelines

DDRII Signal Groups

Group	Signal Name	Length Matching and Length Formulas
Data	SA_DQ[63..0]/SB_DQ[63..0] SA_DQS[7..0]/SB_DQS[7..0] SA_DQSI[7..0]/SB_DQSI[7..0] SA_DQSI[7..0]/SB_DQSI[7..0]	Signal Group Control-to-Clock Command-to-Clock Strobe-to-Clock Data-to-Strobe
Address	SA_A[11..0]/SB_A[11..0] SA_A[11..0]/SB_A[11..0] SA_A[11..0]/SB_A[11..0] SA_A[11..0]/SB_A[11..0]	Minimum Length Clock - 1.0" Clock - 0.0" Clock - 1.0" Clock - 1.0"
Control	SA_CS[3..0] SA_CAS[3..0] SA_ODT[3..0]	Maximum Length Clock - 0.0" Strobe - 220mils Strobe - 180mils
Clock	SA_CLK[3..0] SA_CLK[3..0]	
Feedback	SA_RCVENOUT[7..0]/SB_RCVENOUT[7..0] SA_RCVENIN[7..0]/SB_RCVENIN[7..0]	

CLK group : SM\_CK[3..0],SM\_CKQ[3..0]

Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	55 +/- 15%
Differential Mode Impedance	70 +/- 20%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 8 mils
Nominal CK to CKQ Spacing (edge to edge)	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Serpentine Spacing	Inner Layer : 16 mils Outer Layer : 20 mils
Minimum Spacing to Other DDR2	25 mils
Minimum Isolation Spacing to non-DDR2	750 mils +/- 200 mils
Package Length P1	Max = 50 mils (Escape)
Trace Length Limit - L0	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1	Max = 5000 mils
Maximim Via Count	2 (Per side)
SCR to SCR Length Matching (Total Length including packages)	Match total length to within 5 mils
Clock to Clock Length Match (Total Length)	Match Channel A clocks to X0 +/- 20mils Match Channel B clocks to X1 +/- 20mils
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4/12 mils to other DDR2 Outer Layer : 5/15 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	CK to CKQ spacing rule waived at connector spacing of 15 mils to other DDR2 Max. breakin length is 200 mils

Feedback group : SA\_RCVENIN[7..0],SA\_RCVENOUT[7..0],SB\_RCVENIN[7..0],SB\_RCVENOUT[7..0]

These signals are routed internally on the GMCH package and don't require any routing on the MB. As a result, can be left as INC.

Control group : SM\_CKE[3..0],SM\_CSQ[3..0],SM\_ODT[3..0]

Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 8 mils
Minimum CTRL Trace Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 200 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCR/CKQ Length Matching (Total Length including packages)	(CLK-1.0") +/- CTRL +/- (CLK-0.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Command group : SA\_MA[13..0],SB\_MA[13..0],SA\_BSP[2..0],SB\_BSP[2..0],SA\_RAS#,SB\_RAS#,SA\_CAS#,SB\_CAS#,SA\_WE#,SB\_WE#

Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 8 mils
Minimum CMD Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 200 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCR/CKQ Length Matching (Total Length including packages)	(CLK-1.0") +/- CMD +/- (CLK-1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Data group : SA\_DQ[63..0],SB\_DQ[63..0],SA\_DM[7..0],SB\_DM[7..0]

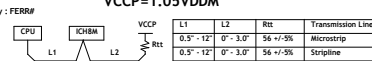
Topology	Point-to-Point
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 8 mils
Minimum DQ Bus Trace Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Serpentine Spacing	Same as DQ-to-DQ routing
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Maximim Via Count	2
DQ/DIM to DQS Length Matching (Total Length including packages)	Match DQ/DIM to (DQS - 200mils) +/- 20mils, per byte lane
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Data Strobe group : SA\_DQS[7..0],SA\_DQS[7..0],SB\_DQS[7..0],SB\_DQS[7..0]

Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	55 +/- 15%
Differential Mode Impedance	85 +/- 20%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 8 mils
Nominal DQS to DQS# Spacing (edge to edge)	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQS to DQ Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Serpentine Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length Range - P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Maximim Via Count	2 (Per side)
DQS to DQS# Length Matching (Total Length including packages)	Match total length to within 5 mils
Clock to Clock Length Match (Total Length including packages)	(CLK-0.5") +/- DQS +/- (CLK-1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 8 mils to other DDR2 Outer Layer : 10 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	DQS to DQS# spacing rule waived at connector spacing of 10 mils to other DDR2 Max. breakin length is 200 mils

VCCP=1.05VDD

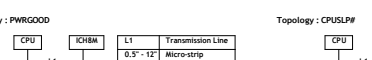
Topology : FERRIF



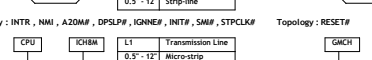
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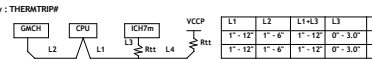
Topology : INTR, NMI, AZDMM, DPSLP#, ICKNE#, INT#, SM#, STPLCK#



Topology : RESE#



Topology : THERMTRIP#



Processor ITP Signal Default Strapping When ITP-XDP & ITP700FLEX Dedbug Port Not Used.

Signal	Resistor Value	Connect To	Resistor Placement
TDI	54.9 OHM +/-5%	VCCP	Within 2.0" of the CPU
TMS	54.9 OHM +/-5%	VCCP	Within 2.0" of the CPU
TRST#	649 OHM +/-5%	GND	Within 2.0" of the CPU
TCK	54.9 OHM +/-5%	GND	Within 2.0" of the CPU
TDO	OPEN	NC	N/A

FSB Common Clock Signal Layout Guide :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
ADSP#, BNSP#, BPSIP#, BROSP#, DBSP#, DEFERR#, DPWRP#, DRDY#, HTM#, HTMP#, LOCKP#, RS2P#, DWP#, TDYVP#, RESE#	Strip-line(Int. Layer)	1.0 - 6.5 inch	55 +/-15%	4 & 8 mils
	Micro-strip(Ext. Layer)			5 & 10 mils

FSB Source Synchronous Data Length Variation and Strobe Matching Requirements :

Signal Name	Signal Matching	Strobes associated with the group	Strobe-to-Strobe Complement Matching
DATA#(15..0), DINVP#	+/- 100 mls	DSTBP0#, DSTBN0#	+/- 25 mls
DATA#(31..16), DINVP#	+/- 100 mls	DSTBP1#, DSTBN1#	+/- 25 mls
DATA#(47..32), DINVP#	+/- 100 mls	DSTBP2#, DSTBN2#	+/- 25 mls
DATA#(63..48), DINVP#	+/- 100 mls	DSTBP3#, DSTBN3#	+/- 25 mls

FSB Source Synchronous Data Signal Routing Topology#1 :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)
DINVP#(3..0)	Strip-line	0.5 - 5.5 inch	55 +/-15%	4 B 8 mils
DATA#(63..0)	Strip-line	0.5 - 5.5 inch	55 +/-15%	4 B 8 mils
DSTBN#(3..0)	Strip-line	0.5 - 5.5 inch	55 +/-15%	4 B 12 mils
DSTBP#(3..0)	Strip-line	0.5 - 5.5 inch	55 +/-15%	4 B 12 mils

FSB Source Synchronous Address Length Variation and Strobe Matching Requirements :

Signal Name	Signal Matching	Strobes associated with the group	Strobe to Assoc. Address Signal Matching
AR#(31..3), REQ#(4..0)	+/- 200 mls	ADSTB0#	+/- 200 mls
AR#(31..17)	+/- 200 mls	ADSTB1#	+/- 200 mls

\*\*\* No length matching requirements exist between ADSTB0# and ADSTB1#

FSB Source Synchronous Address Signal Routing :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)
Address#(31..3)	Strip-line	0.5 - 6.5 inch	55 +/-15%	4 B 8 mils
REQ#(4..0)	Strip-line	0.5 - 6.5 inch	55 +/-15%	4 B 8 mils
ADSTB#(1..0)	Strip-line	0.5 - 6.5 inch	55 +/-15%	4 B 8 mils

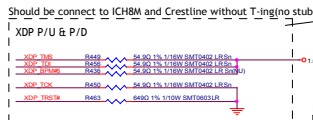
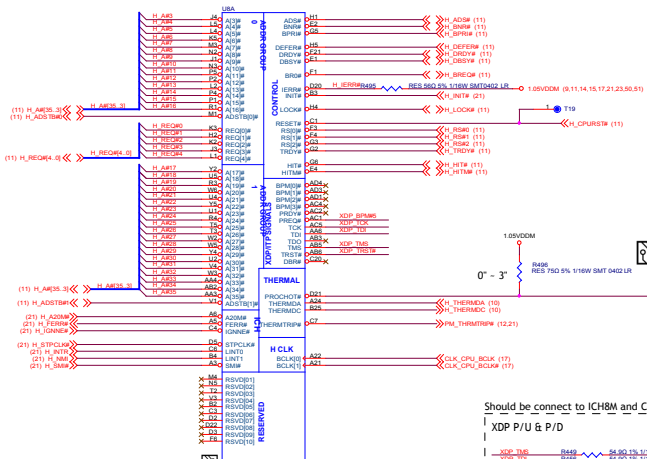
**First International Computer, Inc.**  
 P.O. Box 302, Vero Beach, FL 32980  
 114 Maple, Tallahassee, FL 32304  
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Part: **MR056B**

Doc: **MR056B**

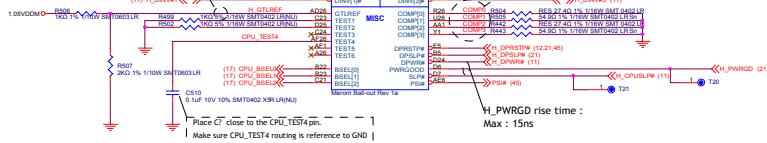
Rev: **1.1**

Date: **11/14/15**



Ar[32-39], APW[0-1]: Leave escape routing on for future functionality

Zo=55ohm, 0.5" max for GTLREF. Space any other switch signals away from GTLREF with a minimum of 25mils. Don't allow the GTLREF routing to create splits or discontinuities in the reference planes of the FSB signals

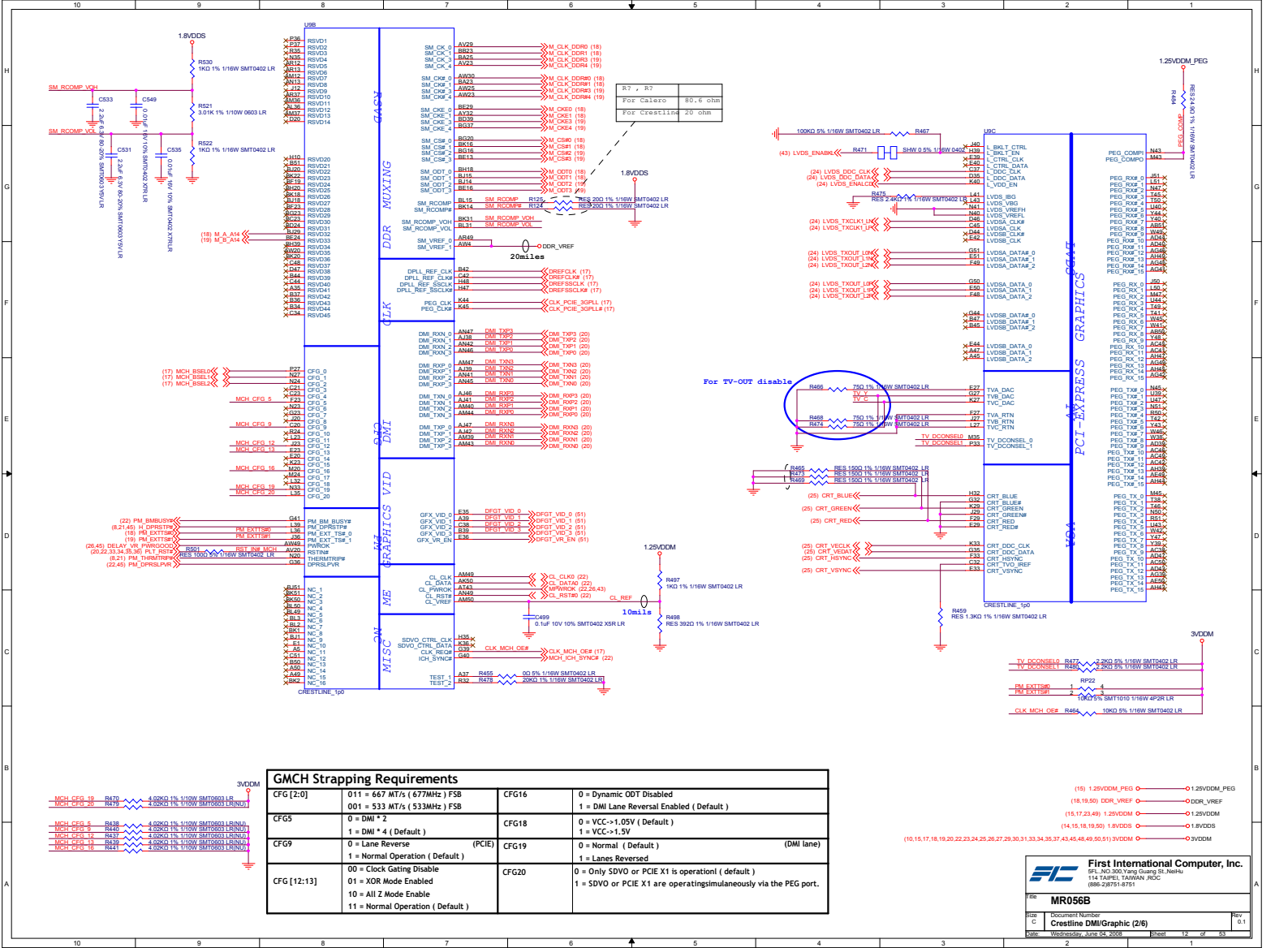


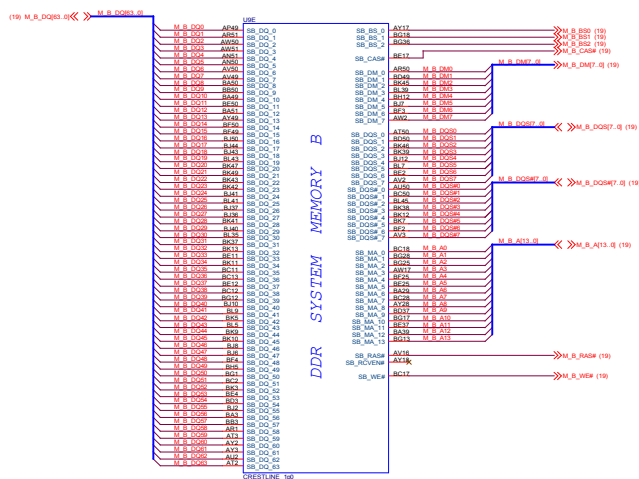


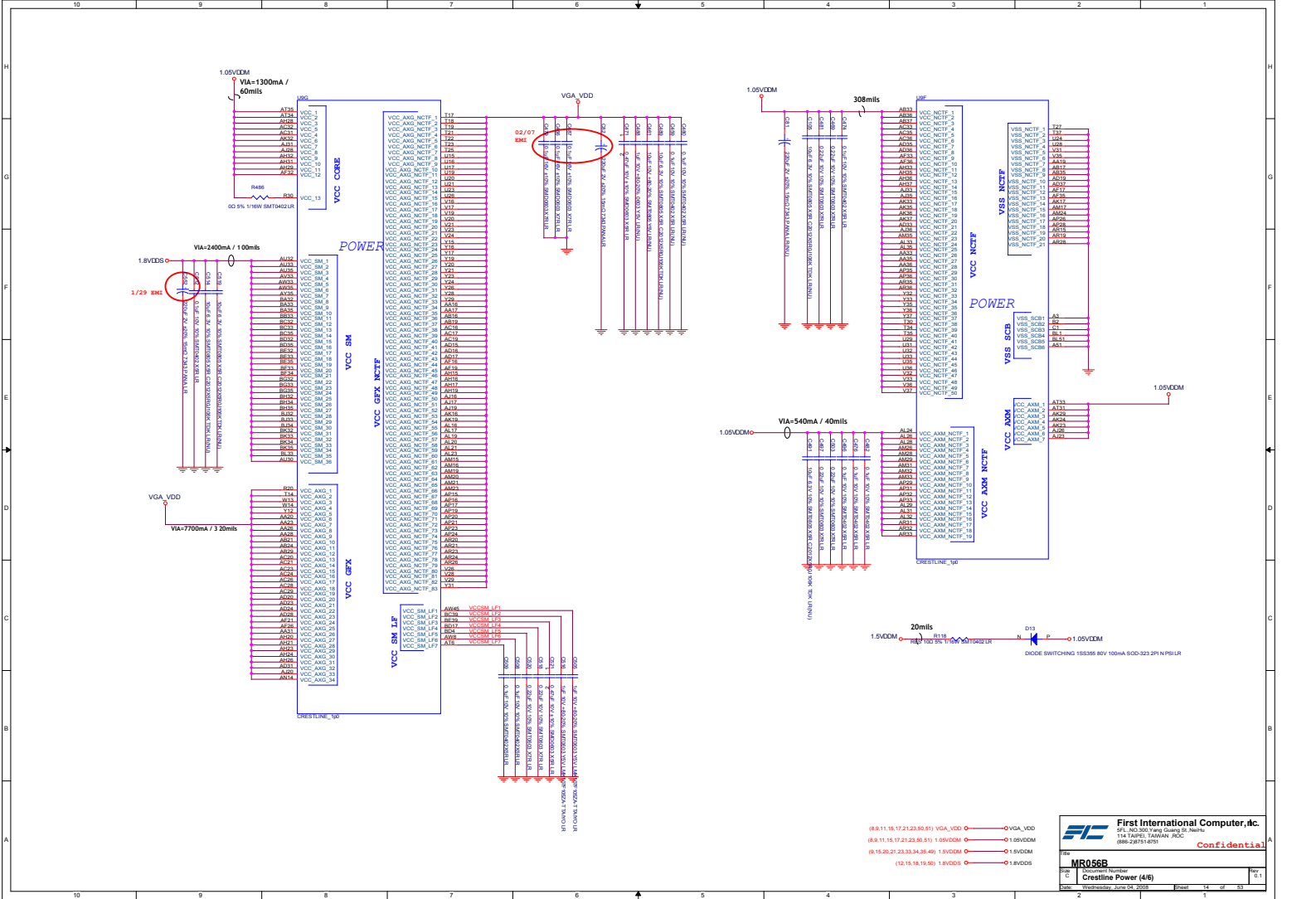


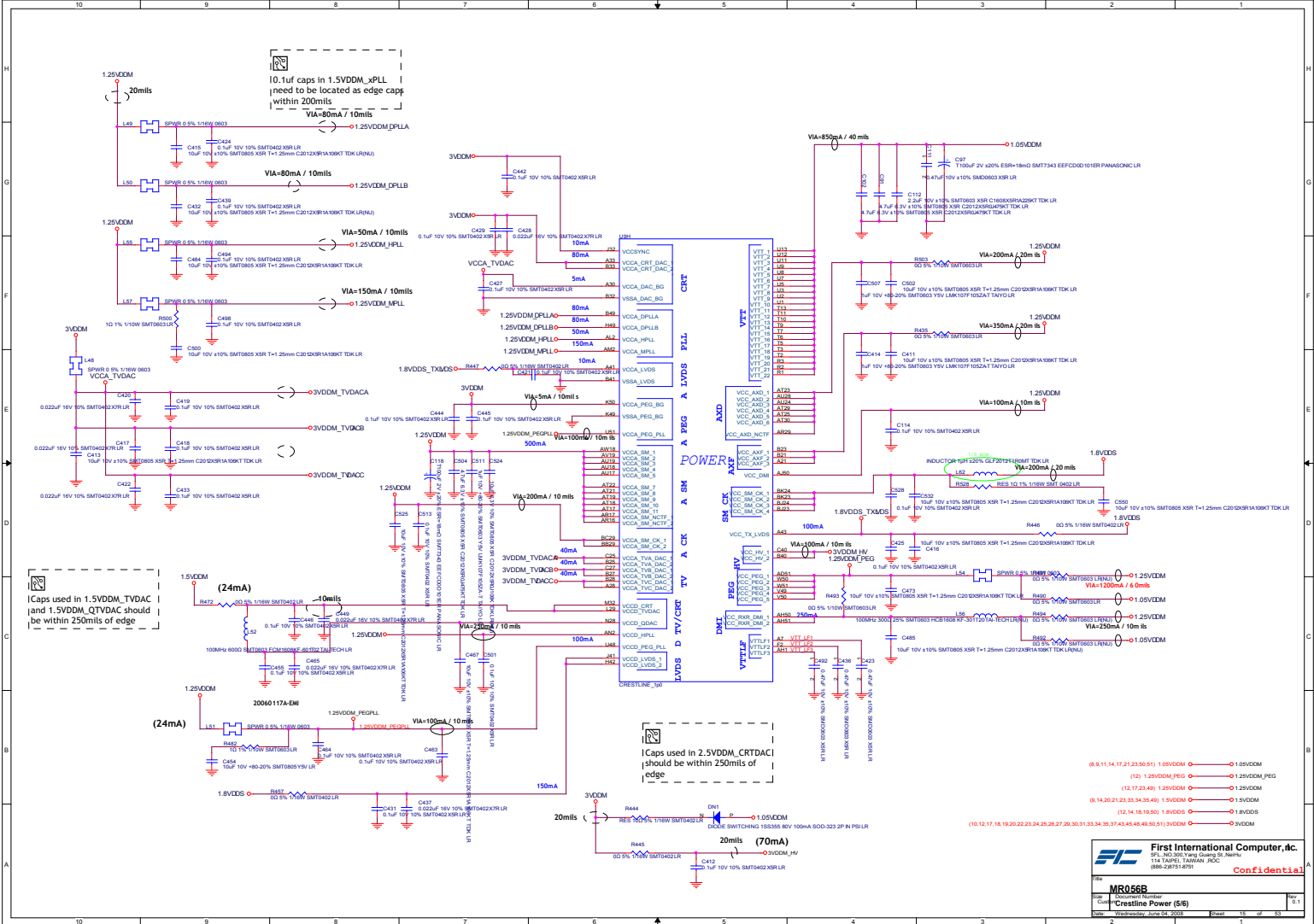






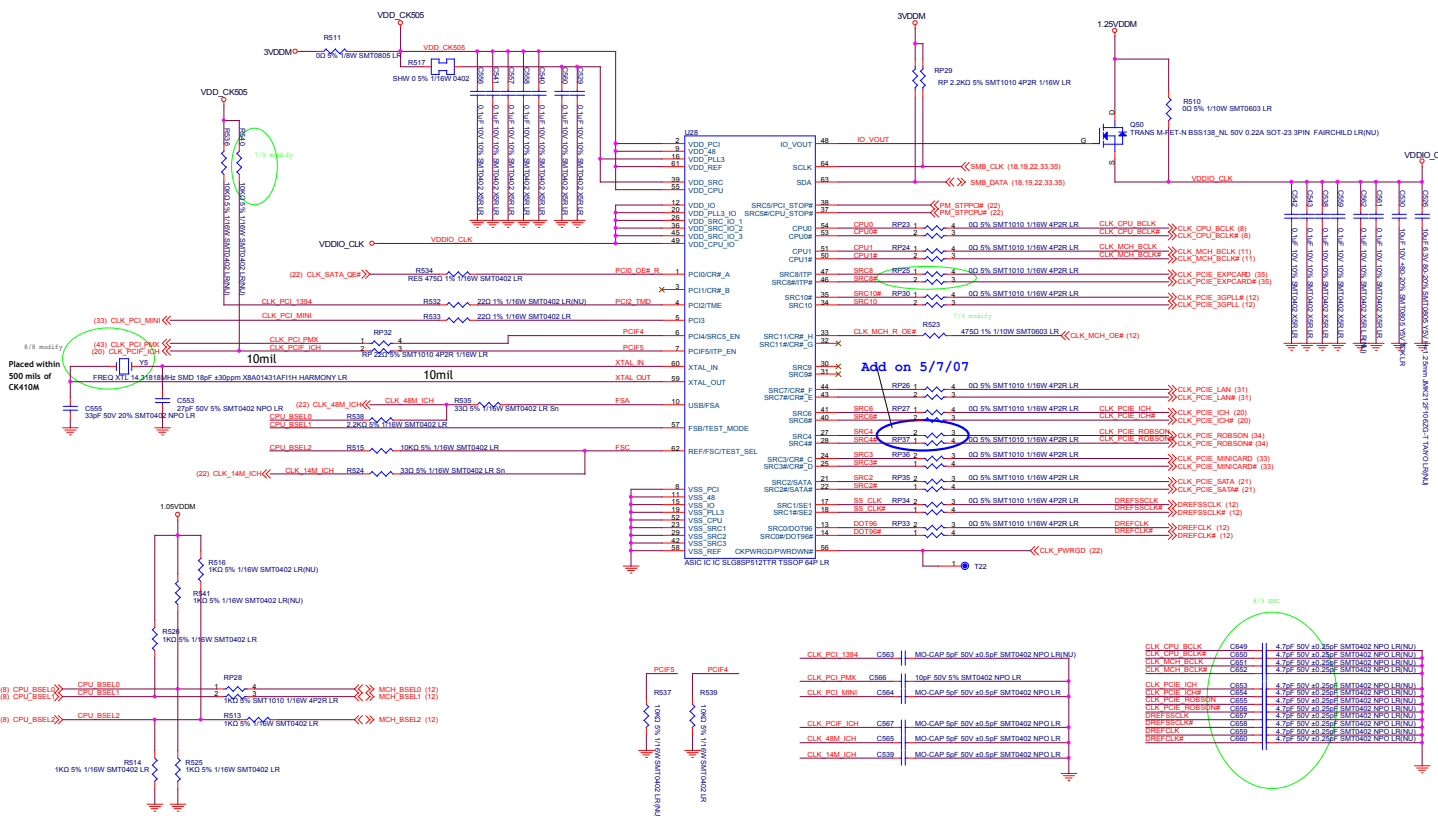












FSC	FSB	FSA	Host Clock
CPU_BSEL2	CPU_BSEL1	CPU_BSEL0	Frequency MHzs
0	1	1	166
0	1	0	200

SS3	SS2	SS1	SS0	Spread Mode	Spread Amount %
0	0	0	0	DOWN	0.8
0	0	0	1	DOWN	1.0
0	0	1	0	DOWN	1.25
0	0	1	1	DOWN	1.5
0	1	0	0	DOWN	1.75
0	1	0	1	DOWN	2.0
0	1	1	0	DOWN	2.5
0	1	1	1	DOWN	3.0

SS3	SS2	SS1	SS0	Spread Mode	Spread Amount %
1	0	0	0	Center	+/- 0.3
1	0	0	1	Center	+/- 0.4
1	0	1	0	Center	+/- 0.5
1	0	1	1	Center	+/- 0.6
1	1	0	0	Center	+/- 0.8
1	1	0	1	Center	+/- 1.0
1	1	1	0	Center	+/- 1.25
1	1	1	1	Center	+/- 1.5

(8,9,11,14,15,21,23,50,51) 1.05VDDM ○ 1.05VDDM  
(12,15,23,49) 1.25VDDM ○ 1.25VDDM  
(10,12,15,18,19,20,22,23,24,25,26,27,29,30,31,33,34,36,37,43,45,46,48,50,51) 3VDDM ○ 3VDDM

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File: **MR056B**

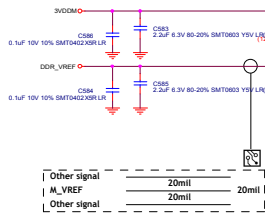
Size: C Document Number: **MR056B**

Rev: 0.1

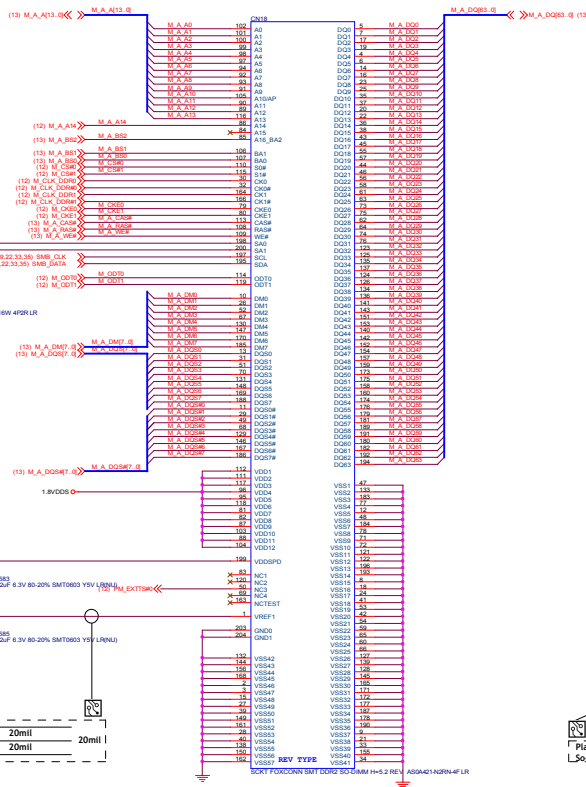
Date: Wednesday, June 24, 2009 Page: 17 of 33

# SO-DIMM0

Note:  
SO-DIMM0 SFD Address is 0xA0  
SO-DIMM0 TS Address is 0x30



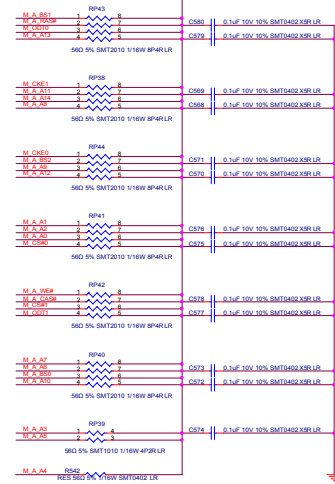
Other signal  
M\_VREF  
Other signal



DDR\_0\_VDD0M

Place one cap close to every 2 pullup resistors terminated to 0.9VDDT\_DDR0

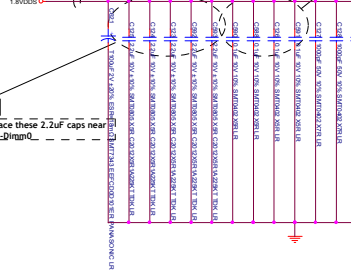
200 mils



Place these resistors near 1 So-Dimm0

Place these 0.1uF caps near 1 So-Dimm0 pin79-pin115 area

160 mils



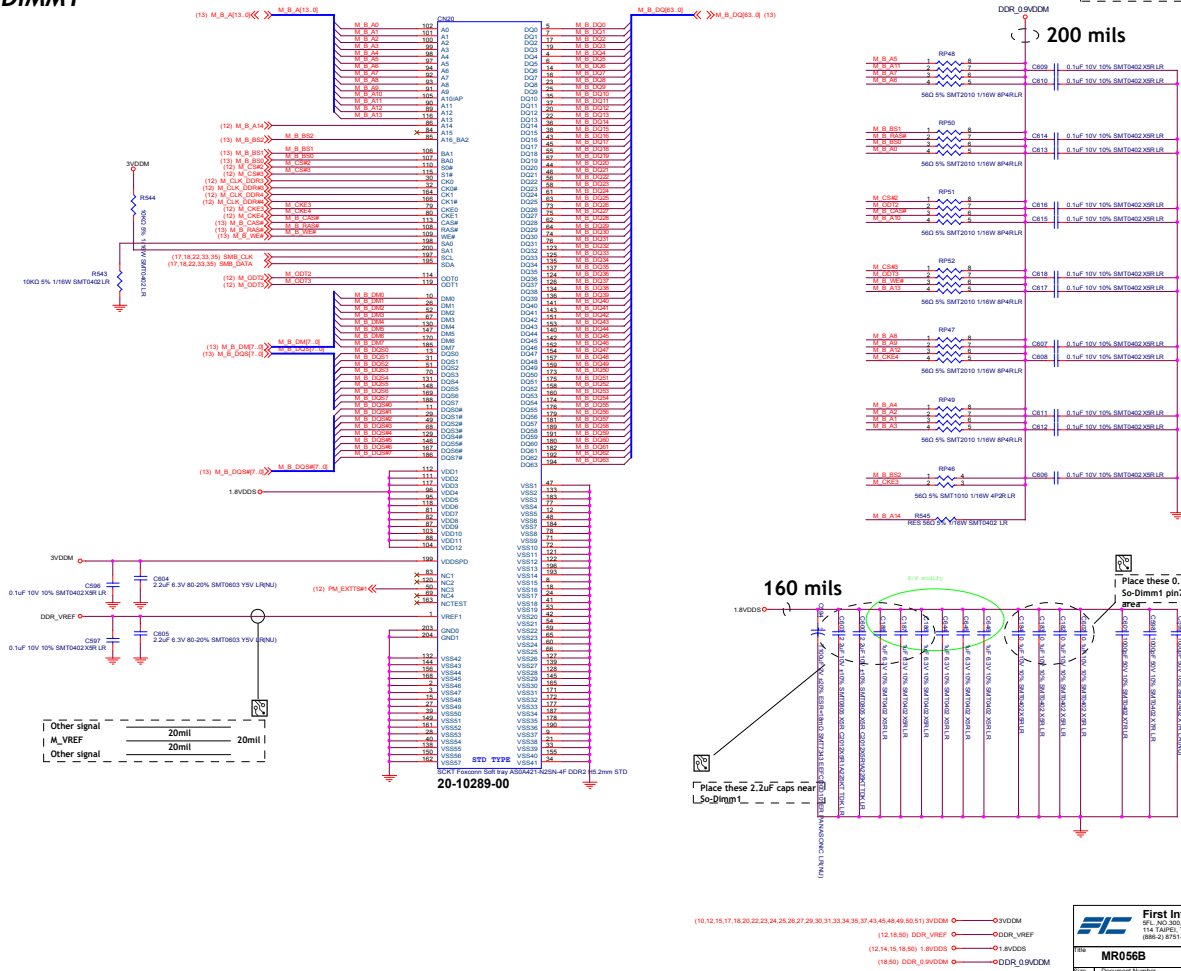
Place these 2.2uF caps near 1 So-Dimm0

(10,12,15,17,18,20,22,23,24,25,26,27,29,30,31,33,34,35,37,43,45,46,49,50,51) VDD0M  
(12,15,50) DDR\_VREF  
(12,14,15,19,50) 1.8VDD0S  
(19,50) DDR\_0\_VDD0M

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114 Capital Mall, Waco, TX 76787-0302  
(800) 251-4351

Part: **MR056B**  
Document Number: **DDR2 SDRAM SO-DIMM0**  
Rev: **0.1**

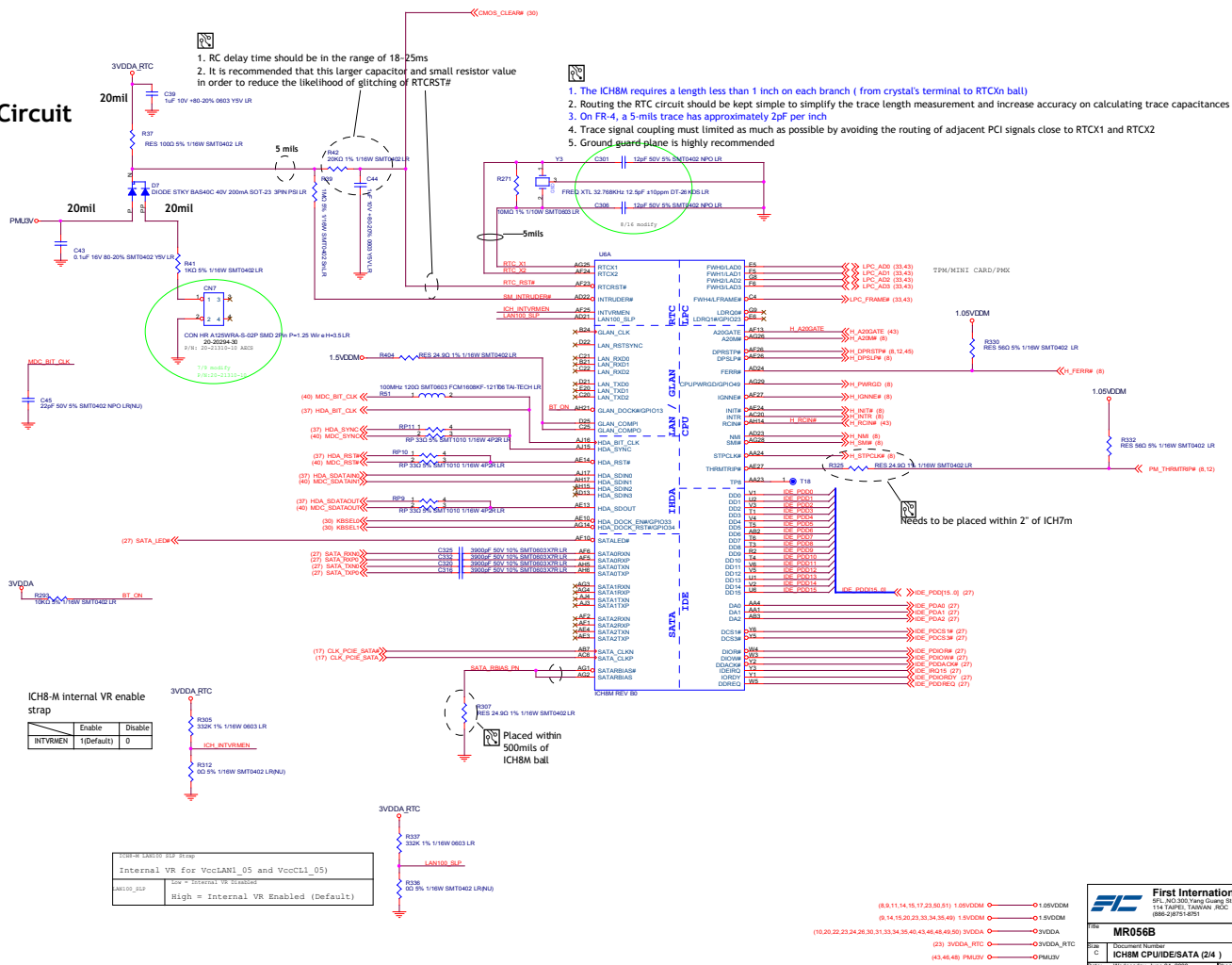
Place one cap close to every 2 pullup resistors terminated to 0.9VDDT\_DDRII



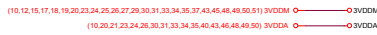
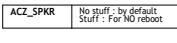
(10,12,15,17,18,20,22,23,24,25,26,27,29,30,31,33,34,35,37,43,45,48,49,50,51) 3VDDM   
(12,18,50) DDR\_VREF   
(12,14,15,18,50) 1.8VDD5   
(18,50) DDR\_0.9VDDM 



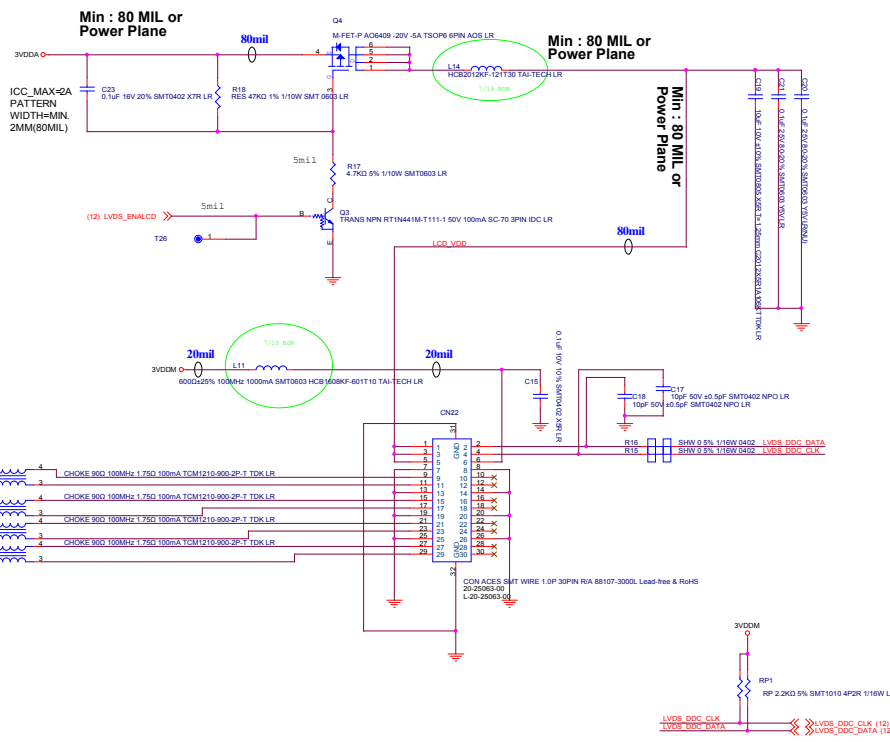
## RTC Circuit



A



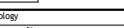




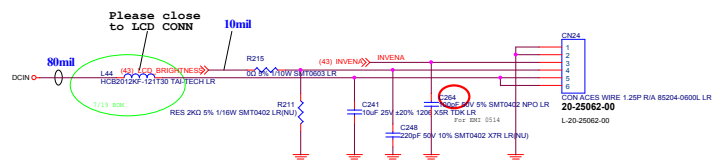
## LVDS Interface

### LVDS Signal Group Routing Guideline

GMCH

	LVDS CN
Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Differential Mode Impedance	100 +/- 20%
Nominal Trace Width	4 mils
Nominal Pair Spacing (Edge to edge)	7 mils
Minimum Pair-to-Pair Spacing	20 mils
Minimum Serpentine Spacing	20 mils
Minimum Spacing to Other LVDS	20 mils
Minimum Isolation Spacing to non-LVDS	20 mils
Maximum Via Count	2 (per line)
Package Length Range - P1	750 mils +/- 250 mils
Total MB Length - TL1	Max = 10"
Length Matching with Pair	Matching to within +/- 20mils
Clock to Data Length Matching (Total Length)	Matching Data to Clock within +/- 20mils
Clock A to Clock B Length Matching	Match Clock A to B within +/- 20mils
Breakout Exceptions (Reduce geometries for GMCH break-out region)	4/4 mils spacing allowed and 10 mils Pair-to-Pair spacing allowed Max. breakout length is 500 mils

\*\*\*Cable Length must be less than 16"

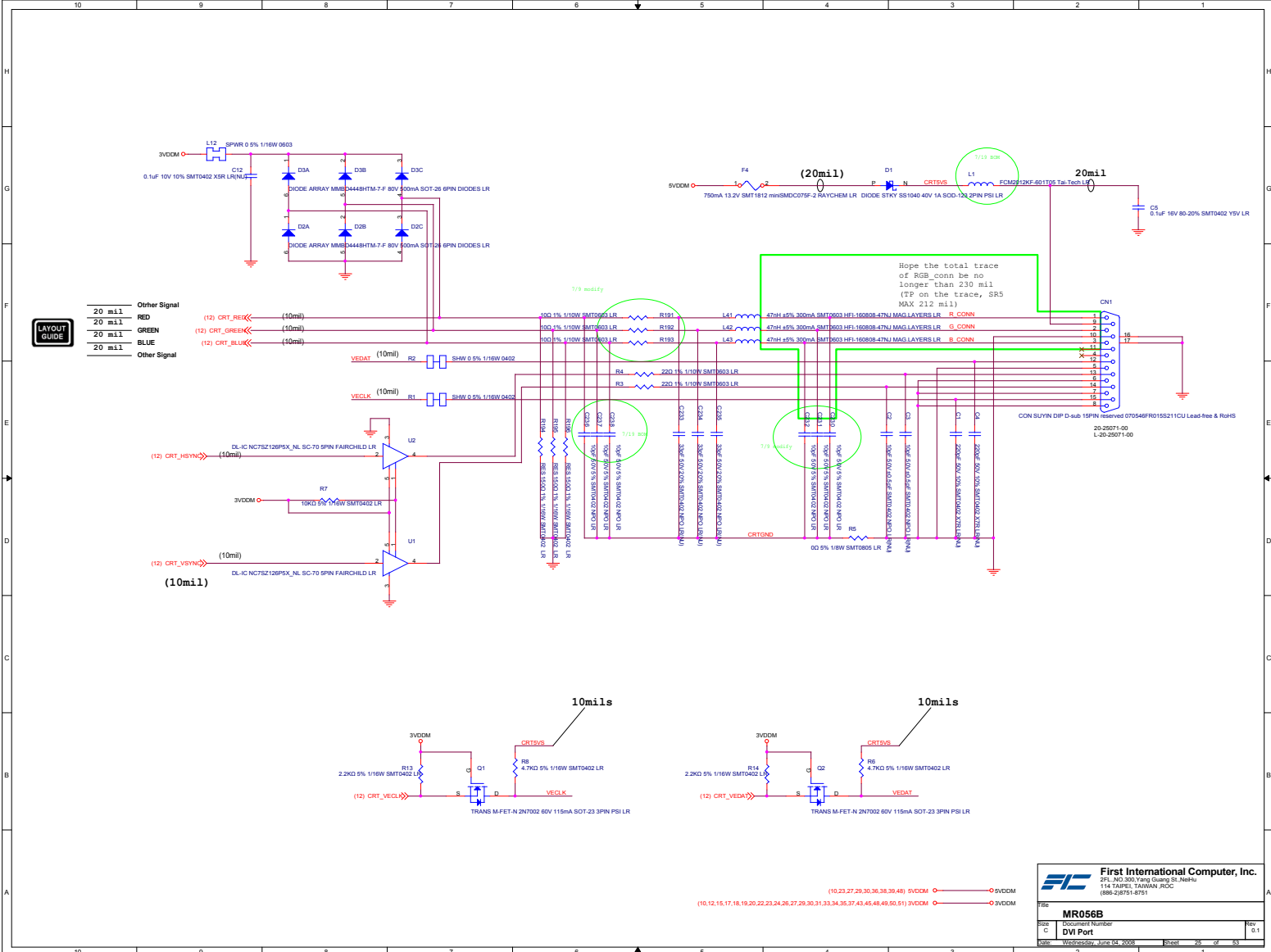


(10,20,21,22,23,25,30,31,33,34,35,40,43,46,48,49,50) 3VDDA ○ 3VDDA  
(10,12,15,17,18,19,20,22,23,25,26,27,29,30,31,33,34,35,37,43,45,48,49,50,51) 3VDDM ○ 3VDDM  
(45,46,47,48,49,50,51) DCIN ○ DCIN

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(886-2)8751-8751

File: **MR056B**  
Size: C Document Number: **LCD CNN** Rev: 0.1  
Date: 10/20/2008 10:00:00 AM 24 of 33





3.3VDC

10 mils

Support power off can flash

0.1uF 10V 10% BMT0402ZGTLR

VDD

VDD1

VDD2

R114 10k

R115 10k

RESET

STM32F402ZGTLR

FLASHROM Serial Flash SPI W25X80VSI (Mbit 2.7V~3.3V C102D088) (8pin) WINBOND LR

C74

10k

STM32F402ZGTLR

SPIN\_B (20)

SPIN\_S0 (20)

SPIN\_S1 (20)

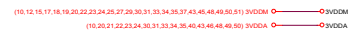
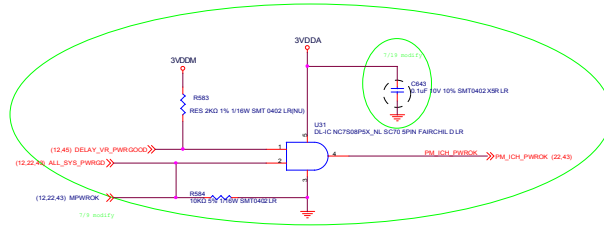
SPIN\_CLK (20)

C75

10k

STM32F402ZGTLR (NPN)

Doc 014



## NOTE

SATA differential stripline 20:5:6:5:20  
SATA differential microstripline 20:6:6:6:20  
請包GROUND

LAYOUT  
GUIDE

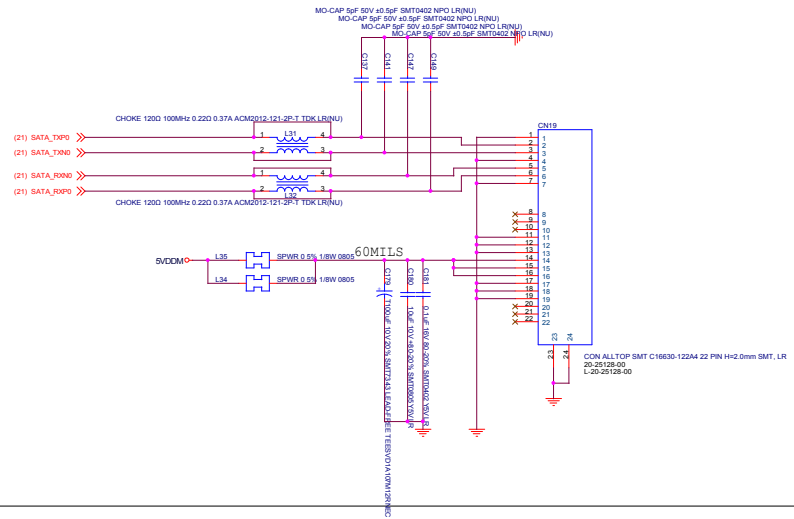
## SATA Layout Note:

MS or SL:

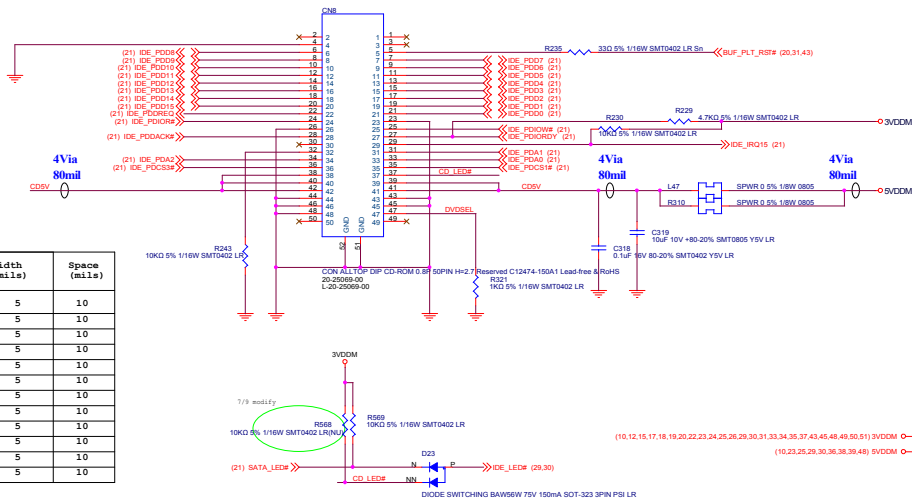
20mils 6mils 6mils 20mils 6mils 6mils 20mils

TX RX

- \* Zdiff = 100 Ohm +/- 10%. TX & RX should refer GND.No via & stubs.The Best layer is Top.
- \* TX/RX trace length < 2 inches.
- \* TX/RX need matching trace  $\pm 10$  mils length.
- \* RX/RX need matching trace  $\pm 10$  mils length.
- \* SATA Pair to Pair Trace matching trace  $\pm 10$  mils length.



## CD-ROM CNN



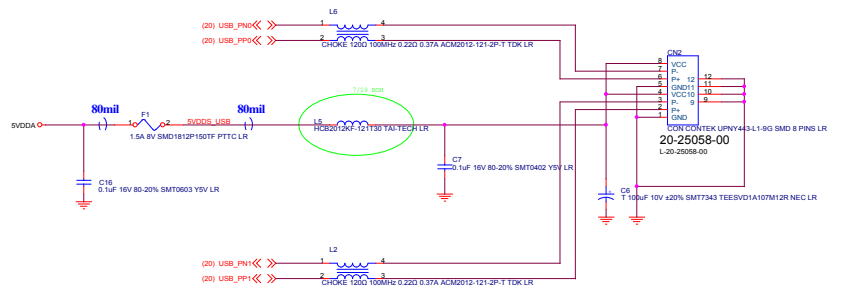
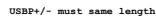
## IDE Signals

Signals	MAX Length (inch)	Width (mils)	Space (mils)
IDE_PDD[15:0]	8	5	10
IDE_SDD[15:0]	8	5	10
IDE_PDA0-2	8	5	10
IDE_SDA0-2	8	5	10
IDE_FDCS 10-30#	8	5	10
IDE_PDRREQ	8	5	10
IDE_SDRREQ	8	5	10
IDE_PDIOW#	8	5	10
IDE_SATADET	8	5	10
IDE_SATADET#	8	5	10
IDE_PDAACK#	8	5	10
IDE_SDAACK#	8	5	10

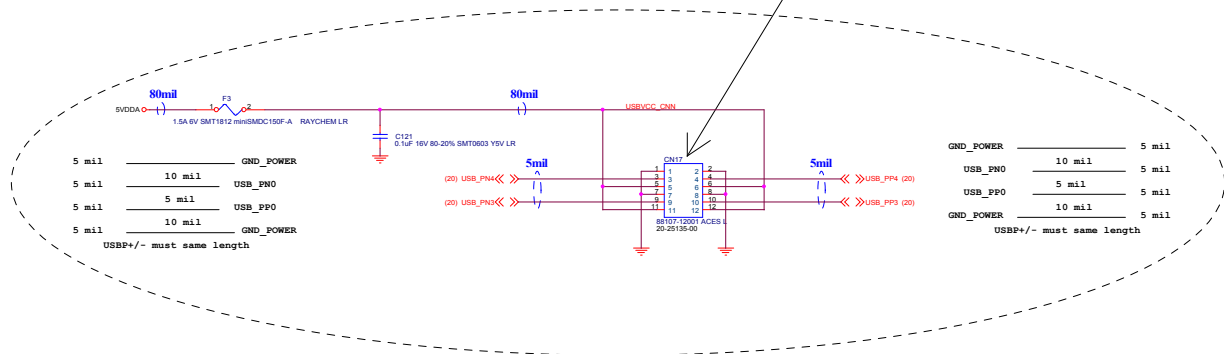
```

5 mil  _____ GND_POWER
          10 mil
5 mil  _____ USB20_P+
          5 mil
5 mil  _____ USB20_P-
          10 mil
5 mil  _____ GND_POWER

```



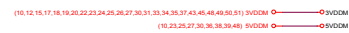
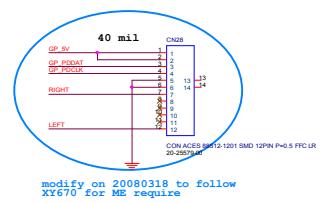
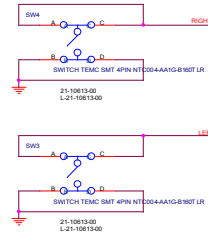
X,Y follow PA354 CN12



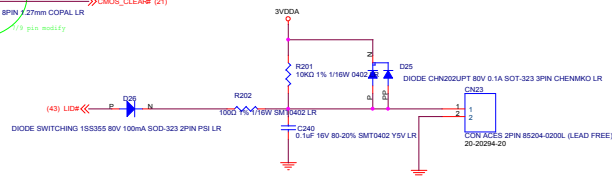
(23,30,45,48,49,50,51) 5VDDA  5VDDA

Signal	Pin
(+3) X0	1
(+3) X1	2
(+3) X2	3
(+3) X3	4
(+3) Y1	5
(+3) Y2	6
(+3) Y3	7
(+3) X4	8
(+3) Y4	9
(+3) X5	10
(+3) Y5	11
(+3) X6	12
(+3) Y6	13
(+3) X7	14
(+3) Y7	15
(+3) X8	16
(+3) Y8	17
(+3) X9	18
(+3) X10	19
(+3) X11	20
(+3) X12	21
(+3) X13	22
(+3) X14	23
(+3) X15	24
(+3) X16	25

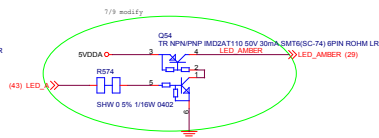
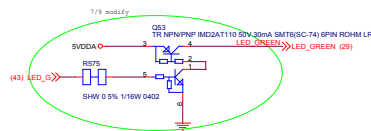
CON/ACE/S/RMT FPC 85002-25022, Lead Free & RoHS  
 20-20088-0  
 L-30-70008-00

[illegible]

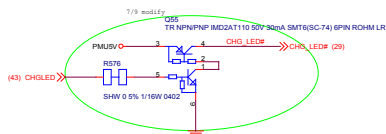
## LID Switch



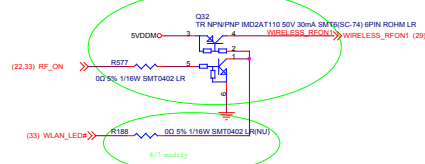
### Power indicator



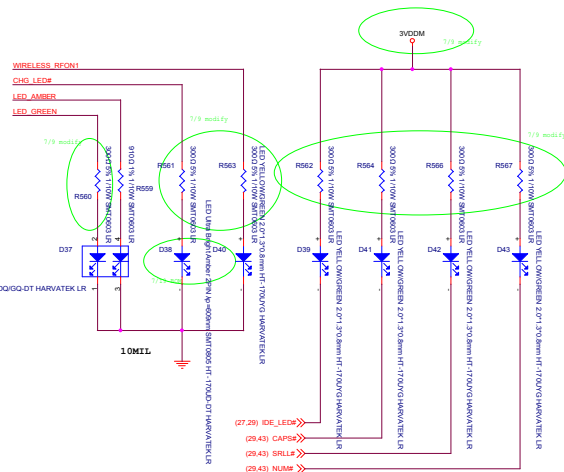
### Charge indicator



### Wireless indicator



### LED indicator control logic



(43,48) PMUSV

(10,20,21,22,23,24,26,31,33,34,35,40,43,46,48,49,50) VDDA

(23,28,45,48,49,50,51) SVDDA

(10,12,15,17,18,19,20,22,23,24,25,26,27,29,31,33,34,35,37,43,45,48,49,50,51) SVDDM

(10,23,25,27,29,36,38,49) SVDDM

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Title	
MR056B	
Size	Document Number
C	LED / SW CN
Date	Wednesday June 04, 2008
Sheet	30 of 63
Rev	0.1

	for 88E8055	for 88E8039
Ra	N.U	Stuff
Rc	4.87K(11-14675-00)	2K(11-14267-00)

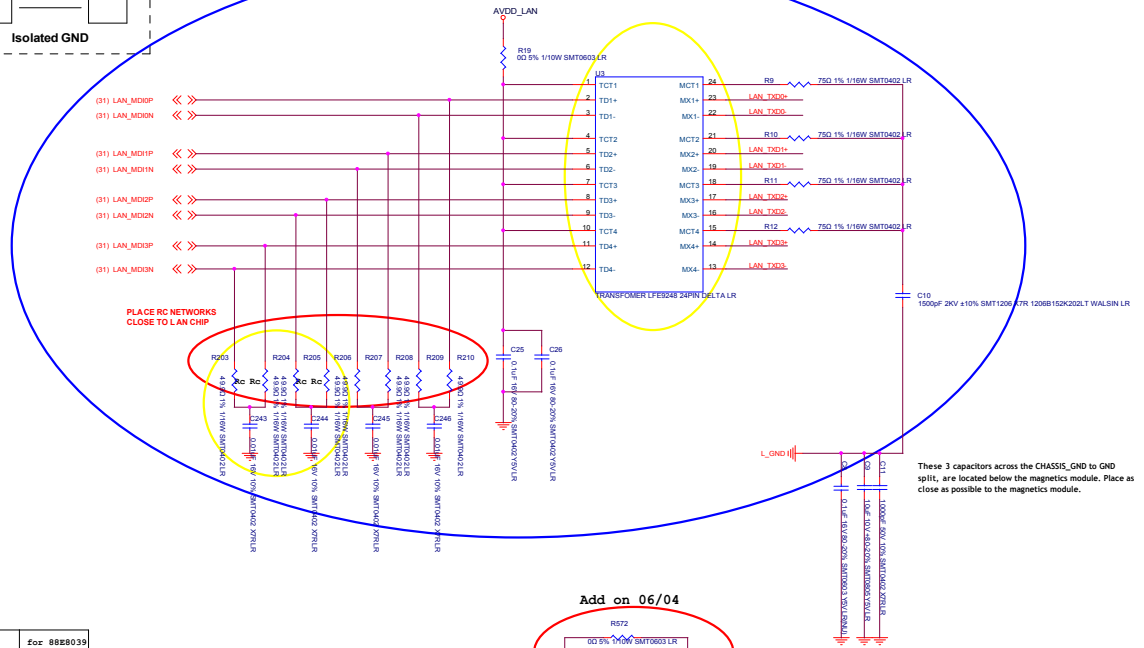


2. The Lan Chip should be placed as close as possible to the transfer.
3. The resistor connected to RSTP pin should be placed near to the Lan Chip, and away from signal traces (RSTP-1) and clock signals as far as possible.
4. The transfer should be placed as close as possible to the R435 connector.
5. The crystal should be placed far away from I/O ports and high frequency signal.
6. The capacitors should be placed as close as possible to the Lan Chip.
7. The decoupling capacitors should be placed as close as possible to the power pins, such that the distance is within 20mil.
8. Traces routed from the Lan Chip to the transfer, and to the R435 connector should be, as short as possible.
9. The distance from maximum length between Lan Chip and transfer is achievable only when there's no interferences around.
10. The R435 and R436 should be placed as close as possible to Lan Chip, and the distance is within 20mil.
11. If power pins are next to each other and there is not much room to accommodate multiple capacitors, then the power pins can share the same capacitors.
12. It's important to separate digital signals from analog pins. If it is unavoidable to cross digital signals with analog power, do it at 90 degree.
13. The digital power plane should be separated from analog areas.
14. The ICs should be placed as close as possible to the IC as possible and the traces should be short.
15. The Lan Chip pin 1 facing the transformer, then you can make the signal shorter.

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Title <b>MR056B</b>		
Size C	Document Number <b>PCIE GIGA LAN PHY 88E8055</b>	Rev 0.1
Date: Wednesday, June 04, 2008		Sheet 31 of 53

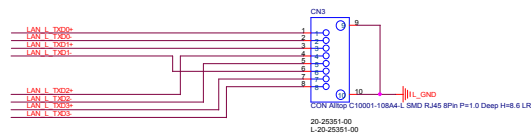
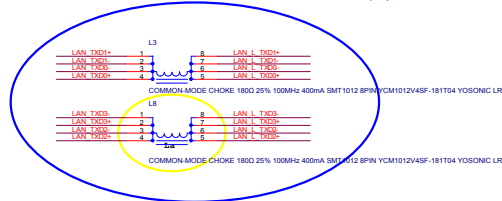
The diagram shows a transformer with a center tap. The primary winding is connected to a 'GND PLANE' through terminals E, 8, 0, and 5. The secondary winding is connected to an 'Isolated GND' through terminals R, J, 4, and 5. The center tap is labeled 'TX+'. The diagram includes labels for 'GND', 'GND PLANE', 'Isolated GND', and 'Transformer'.

Add on 5/7/07



	for 88E8055	for 88E8035
Rc	STUFF	NU
La	STUFF	NU

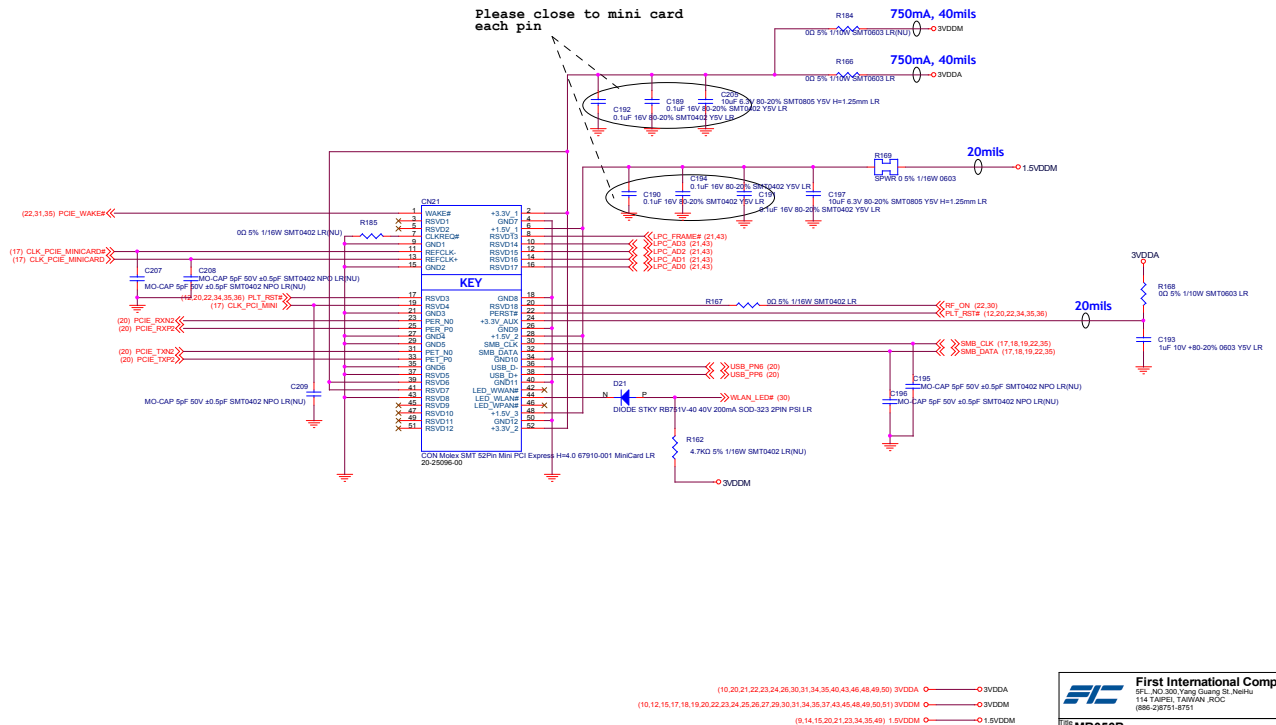
Add on 5/7/07



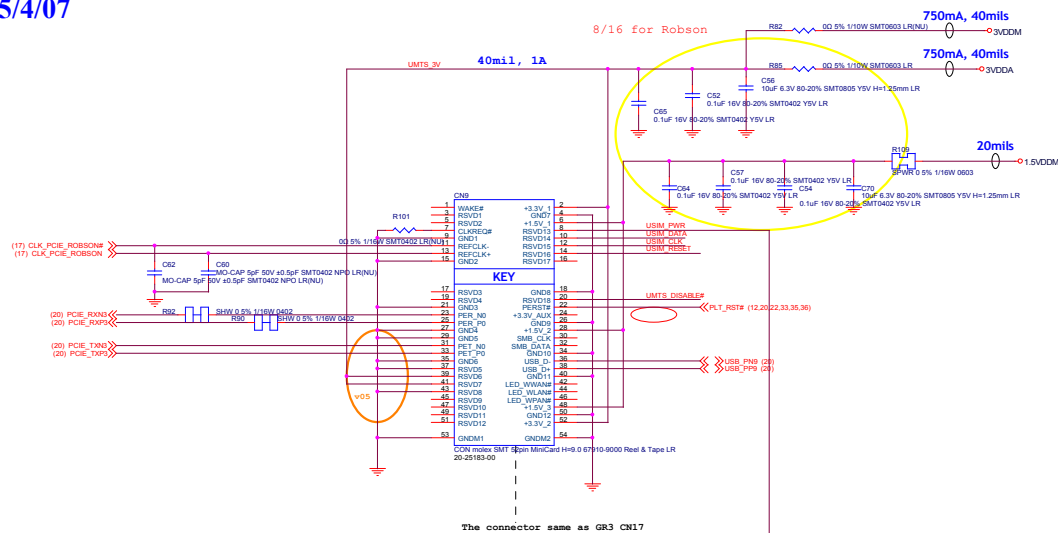
(31) AVDD\_LAN ○ ——— ○ AVDD\_LAN



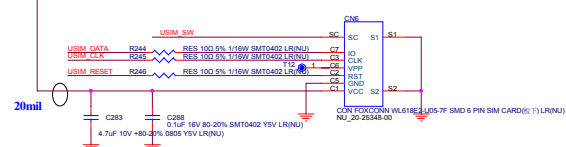
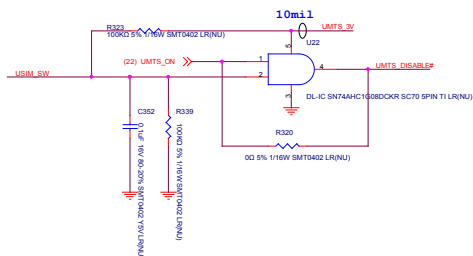
## PCIE Mini Card for Wireless Lan



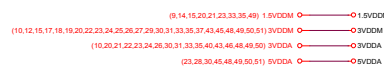
**Robson / UMTS**  
**Add on 5/4/07**



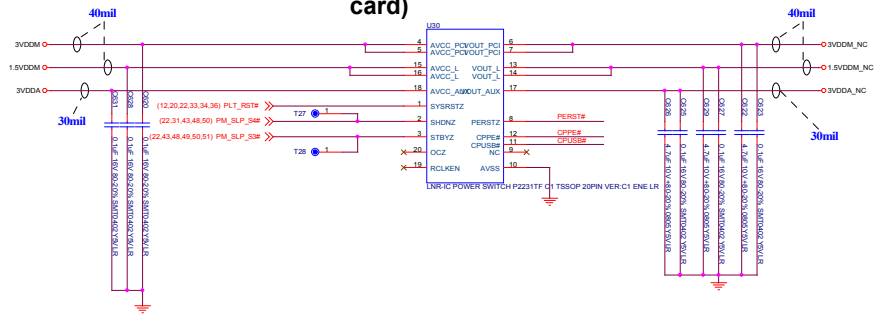
## SIM Card Switch



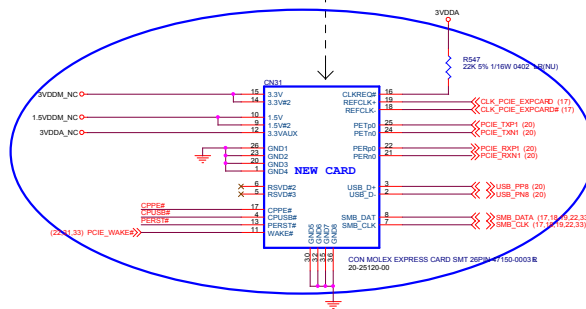
## SIM Card CN



# New Card(express card)



X,Y follow LM10W ME drawing 5/10  
ME engineers need to check

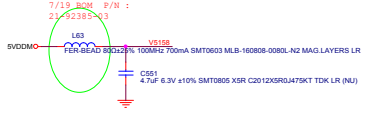
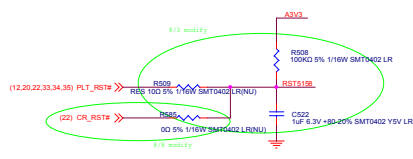
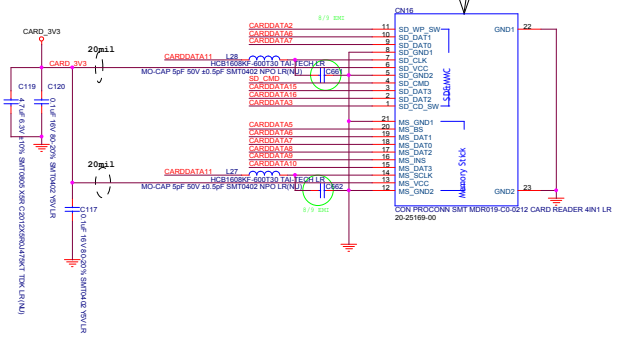
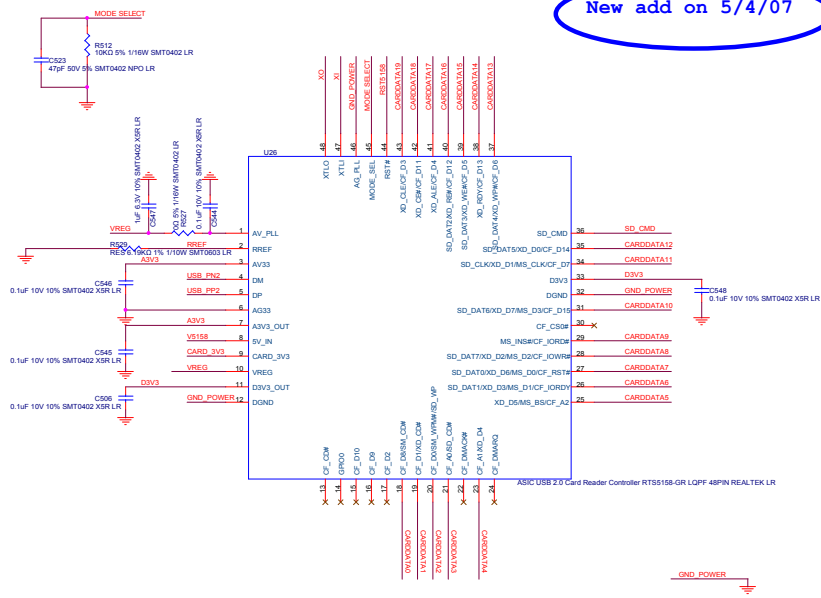


(10,20,21,22,23,24,26,30,31,33,34,40,43,46,48,49,50) 3VDDA  
(9,14,15,20,21,23,33,34,49) 1.5VDDM  
(10,12,15,17,18,19,20,22,23,24,25,26,27,29,30,31,33,34,37,43,45,48,49,50,51) 3VDDM

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Title: <b>MR056B</b>	
Size: C	Document Number: New Card
Rev: 0.1	Rev: 0.1
Date: 2008-04-08	

New add on 5/4/07

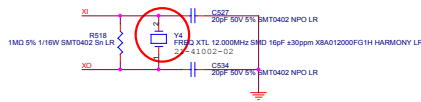
X,Y follow PA354




## INTERFACE



change package on 0525

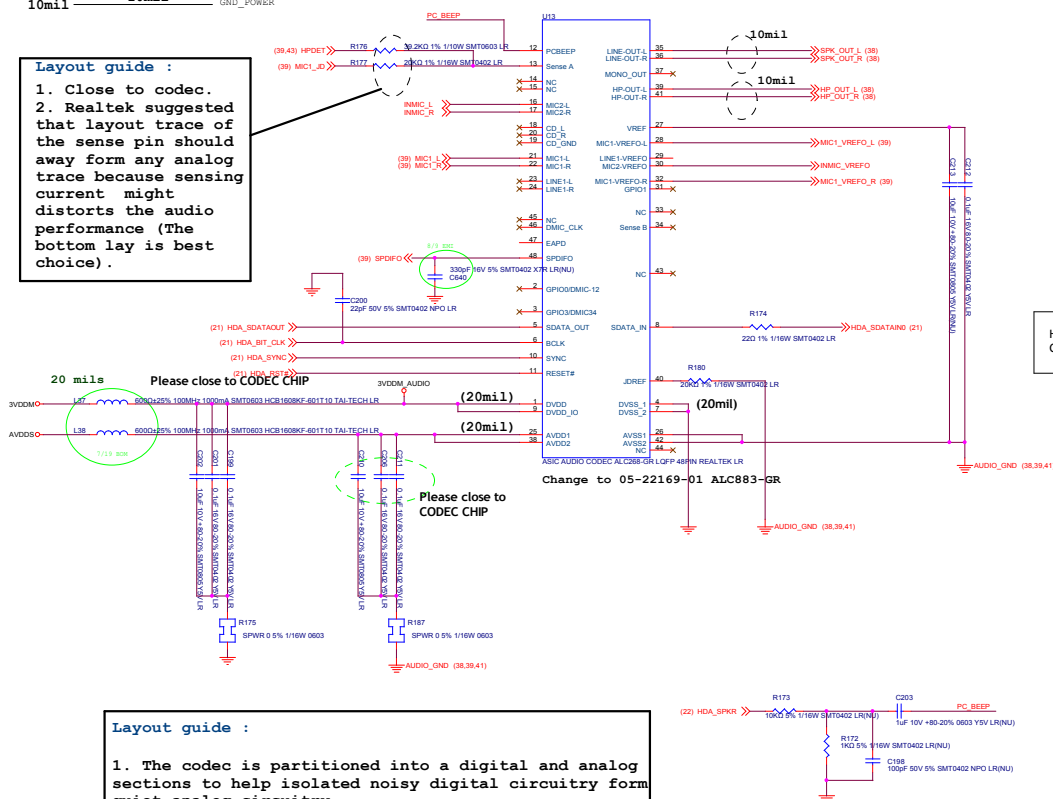


(10,23,25,27,29,30,38,39,48) 5VDDM  5VDDM

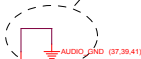
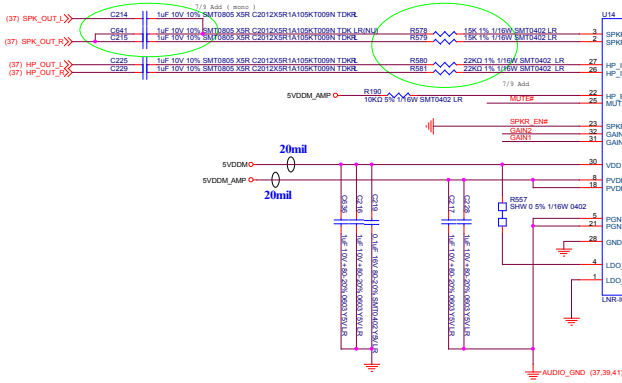
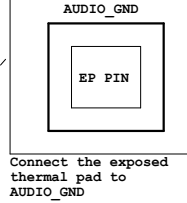
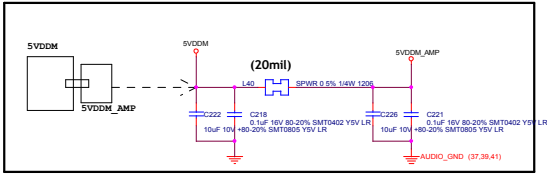
 <b>First International Computer, Inc.</b> 5F, NO.30, Yang Guang St., Ntshih TAIPEI, TAIWAN, R.O.C. (886-2)8751-8751	
Title	
<b>MR056B</b>	
Size	Rev
C	0.1
Document Number	
<b>RTS1558 Card Reader</b>	
Date:	Sheet
Wednesday, June 04, 2008	36 of 53

1. The codec is partitioned into a digital and analog sections to help isolated noisy digital circuitry from quiet analog circuitry.
2. The layout separates the analog and digital planes with a 60 to 100 mils gap and connect them at one point beneath the codec with a 50 mils wide blink.
3. Never route digital traces or digital planes under the analog ground areas. Analog components should be located over analog planes (ground and power planes) and digital components should be located over digital planes.

Change to 05-22169-01 ALC883-GR

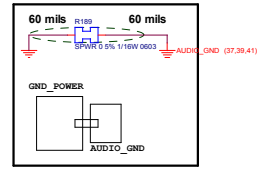
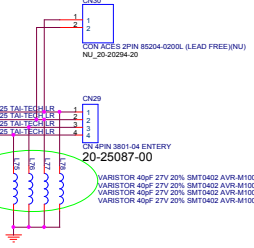


(10,12,15,17,18,19,20,22,23,24,25,26,27,29,30,31,33,34,35,43,45,48,49,50,51) 3VDDM  3VDD



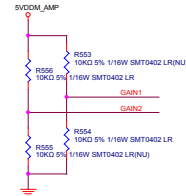
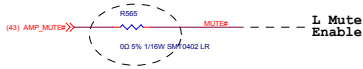
trace 10mil

trace 10mil



SPKR\_EN# = High :Disable Speaker Amplifiers  
HP\_EN = Low :Disable the Headphone Amplifiers

## AMP MUTE#



## Speaker Mode gain (Max)

GAIN1	GAIN2	GAIN
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

(10,12,15,17,18,19,20,22,23,24,25,26,27,29,30,31,33,34,35,37,43,45,48,49,50,51) SVDOM  
(10,23,25,27,29,30,36,39,46) SVDOM  
(37) AVDD5

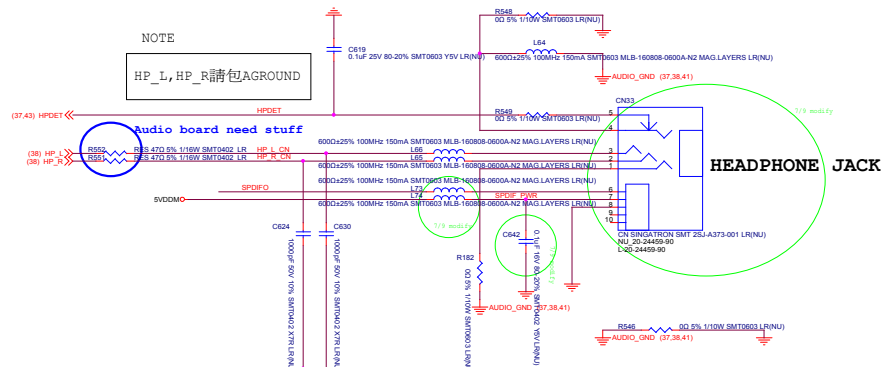
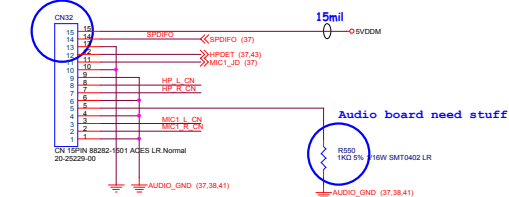
**First International Computer, Inc.**  
2FL, 340-300, Yang Guang St., Neihu  
114 Taipei, TAIWAN, ROC  
(886-2)8751-8751

**MR056B**

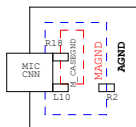
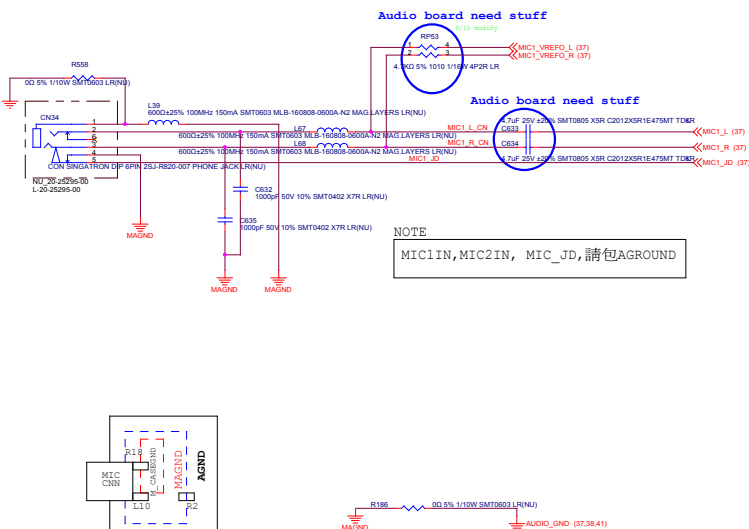
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Document Number: Azalia ALC883GR- Codec  
Rev: 0.1

Date: 2008-06-24, 2008-06-24, 2008-06-24

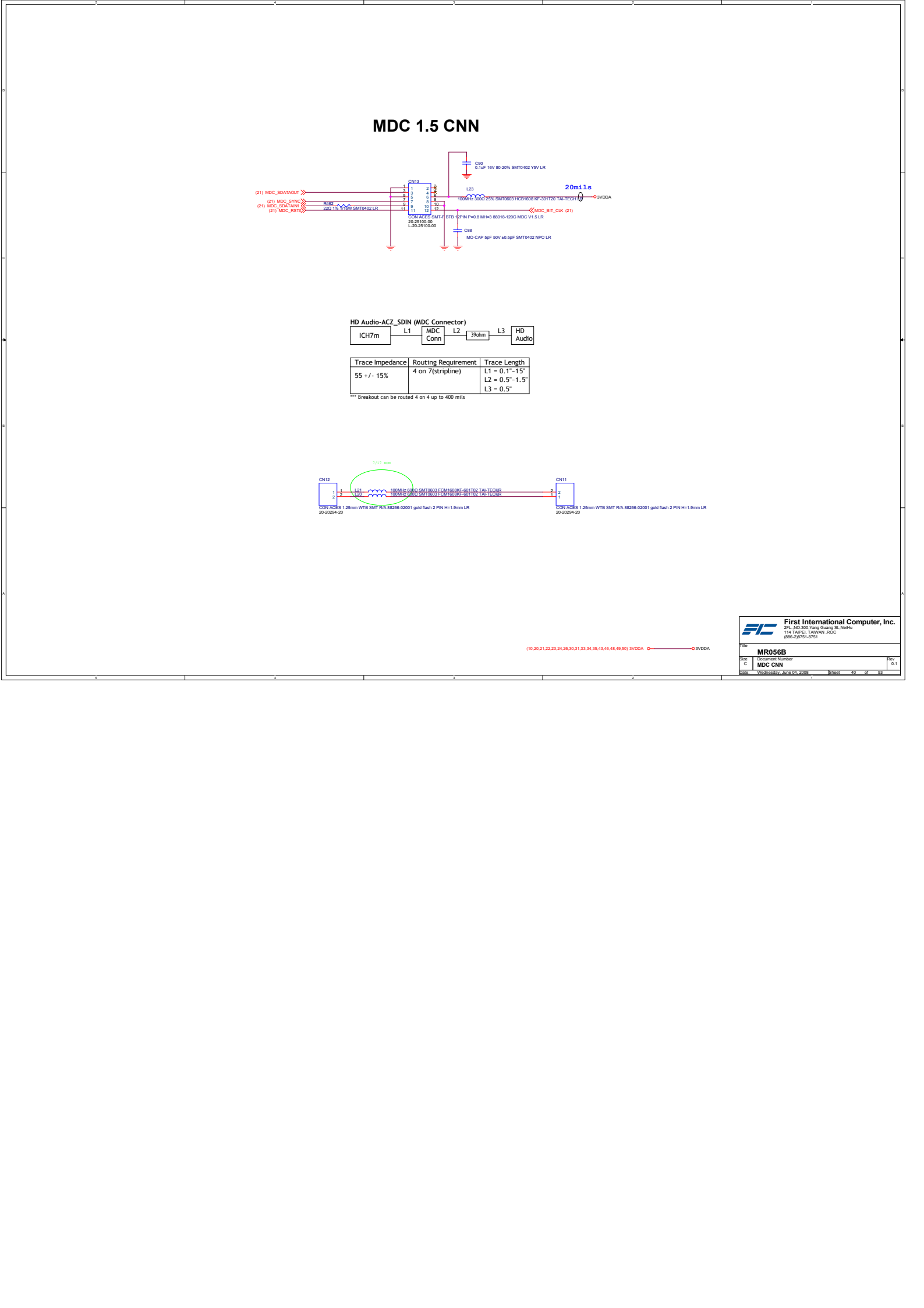
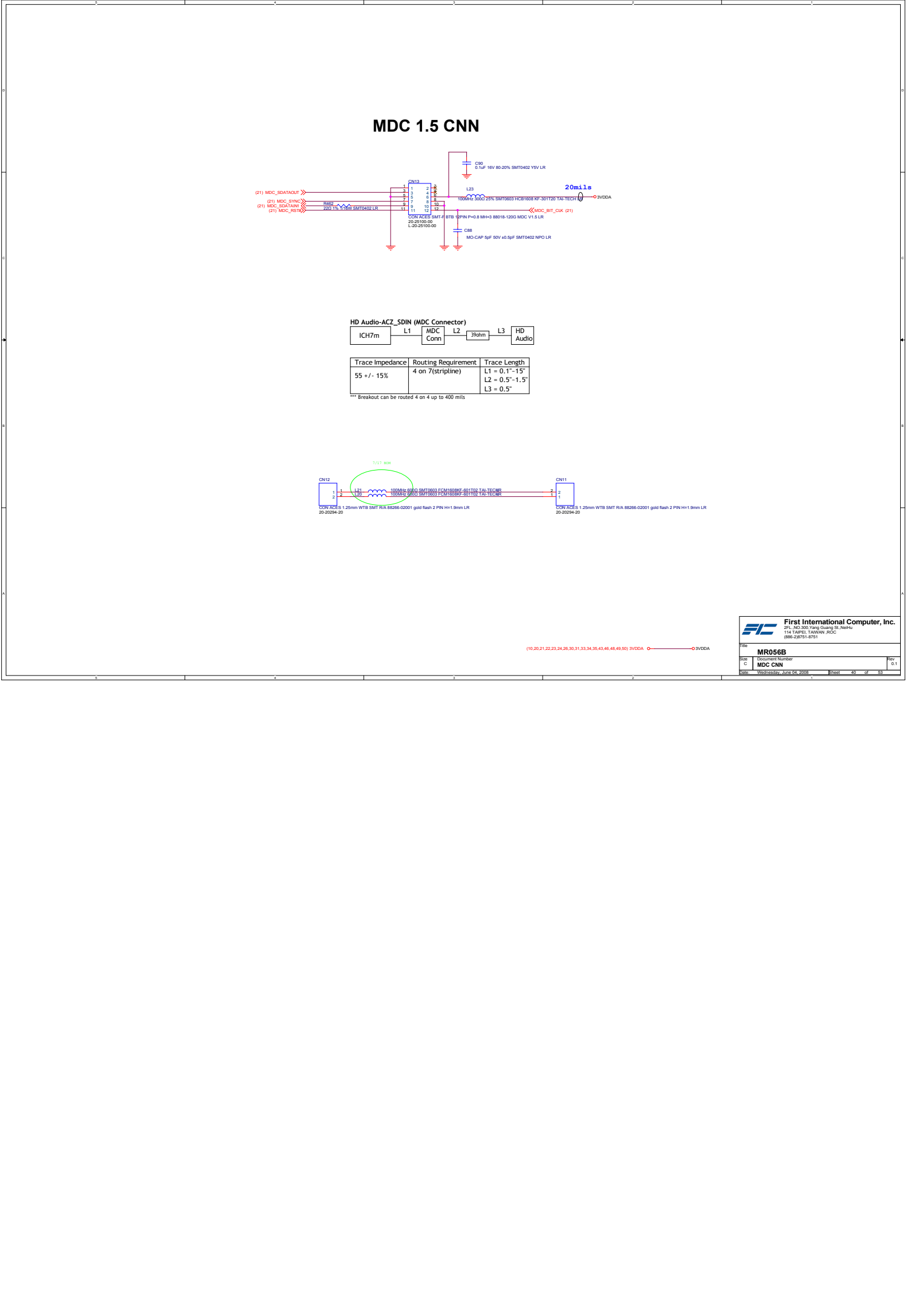
Audio board need stuff



## MIC IN



(10,23,25,27,29,30,36,38,48) 5VDDM  5VDDM

[illegible][illegible]

**MDC 1.5 CNN**

(21) MDC\_SYNC  
(21) MDC\_DATAIN  
(21) MDC\_DATAOUT  
(21) MDC\_BIT\_CLK (21)

C90  
0.1uF 16V 80-20% SMT0402 Y5V LR

L23  
100nH 300Ω 25% SMT0803 HCB1808 RF-351120 TAI-TECH

20mils

3VDDA

CN13

1 2 3 4 5 6 7 8 9 10 11 12

CON ACES SMT-R BTB 10PIN P=0.8 MM H=3.88018-120G MDC V1.5 LR  
20-25100-00  
L-20-25100-00

C98  
MO-CAP 5pF 50V ±0.5pF SMT0402 NPO LR

HD Audio-ACZ\_SDIN (MDC Connector)

ICH7m	L1	MDC Conn	L2	39ohm	L3	HD Audio
-------	----	----------	----	-------	----	----------

Trace Impedance	Routing Requirement	Trace Length
55 +/- 15%	4 on 7 (stripline)	L1 = 0.1"-1.5" L2 = 0.5"-1.5" L3 = 0.5"

\*\*\* Breakout can be routed 4 on 4 up to 400 mils

7/11 30G

CN12

1 2

CON ACES 1.25mm WTB SMT RJA B8266-02001 gold flash 2 PIN H=1.9mm LR  
20-20294-20

L23  
100nH 300Ω 25% SMT0803 HCB1808 RF-351120 TAI-TECH

CN11

1 2

CON ACES 1.25mm WTB SMT RJA B8266-02001 gold flash 2 PIN H=1.9mm LR  
20-20294-20

(10,20,21,22,23,24,26,30,31,33,34,35,43,46,48,49,50) 3VDDA

3VDDA

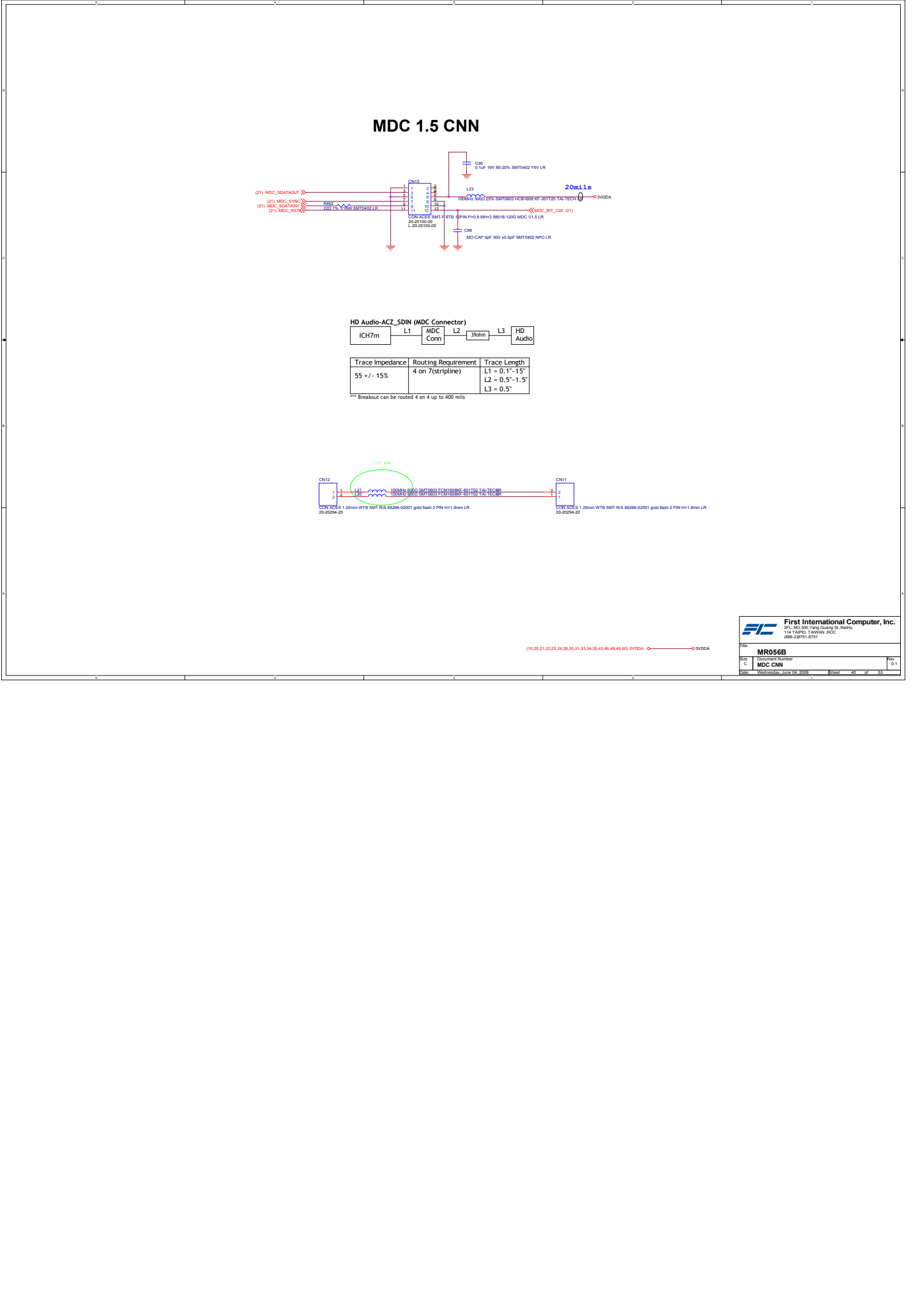
**First International Computer, Inc.**  
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**MR056B**

Document Number  
**MDC CNN**

Rev  
0.1

Issue: Implementation, June 04, 2008, Sheet: 40 of 50



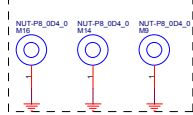


7/9 modify

stuff

P/N:24-10966-51

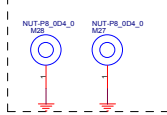
For CPU Heat Sink



stuff

P/N:24-10966-51

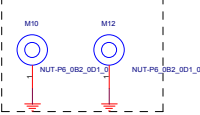
For FAN



stuff

P/N:24-10732-21

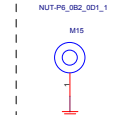
For MDC



stuff

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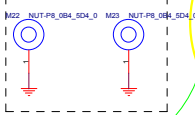
For NB heat sink



stuff

P/N:24-11743-50

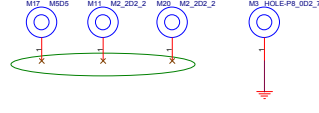
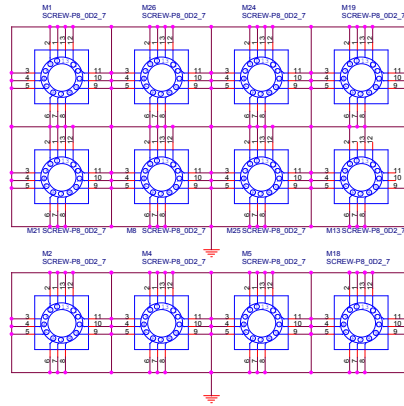
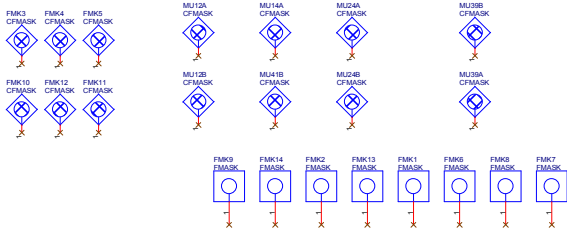
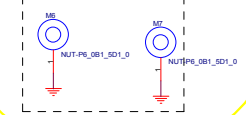
For mini car



Add on 5/7/07

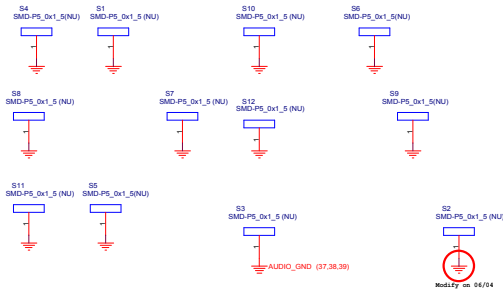
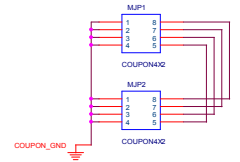
Not stuff 8/16 for Robson  
P/N:24-11618-50

For Robson connector NUT



9/26 Change not connect to GND

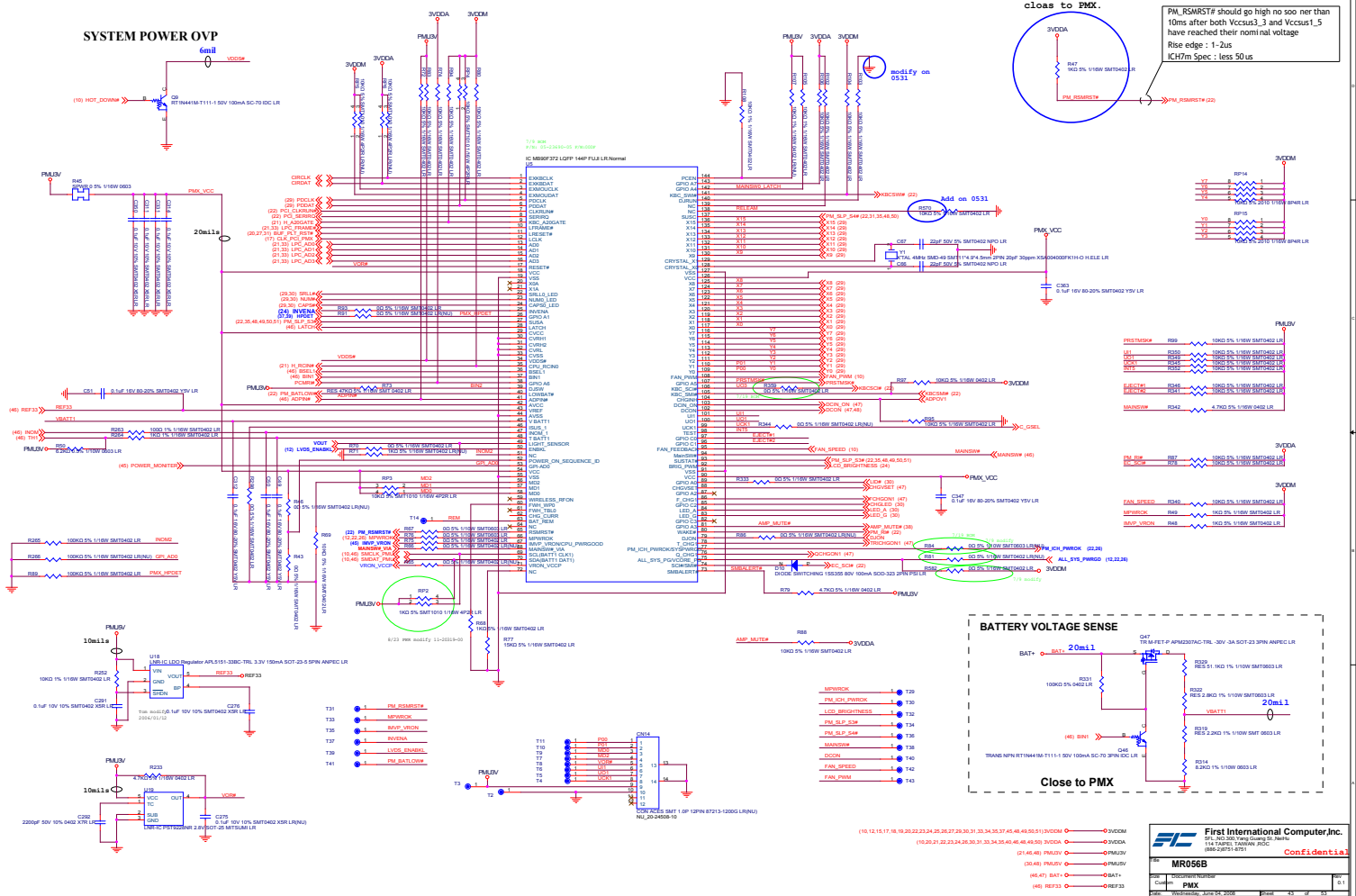
COUPON4X2



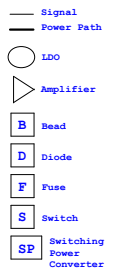
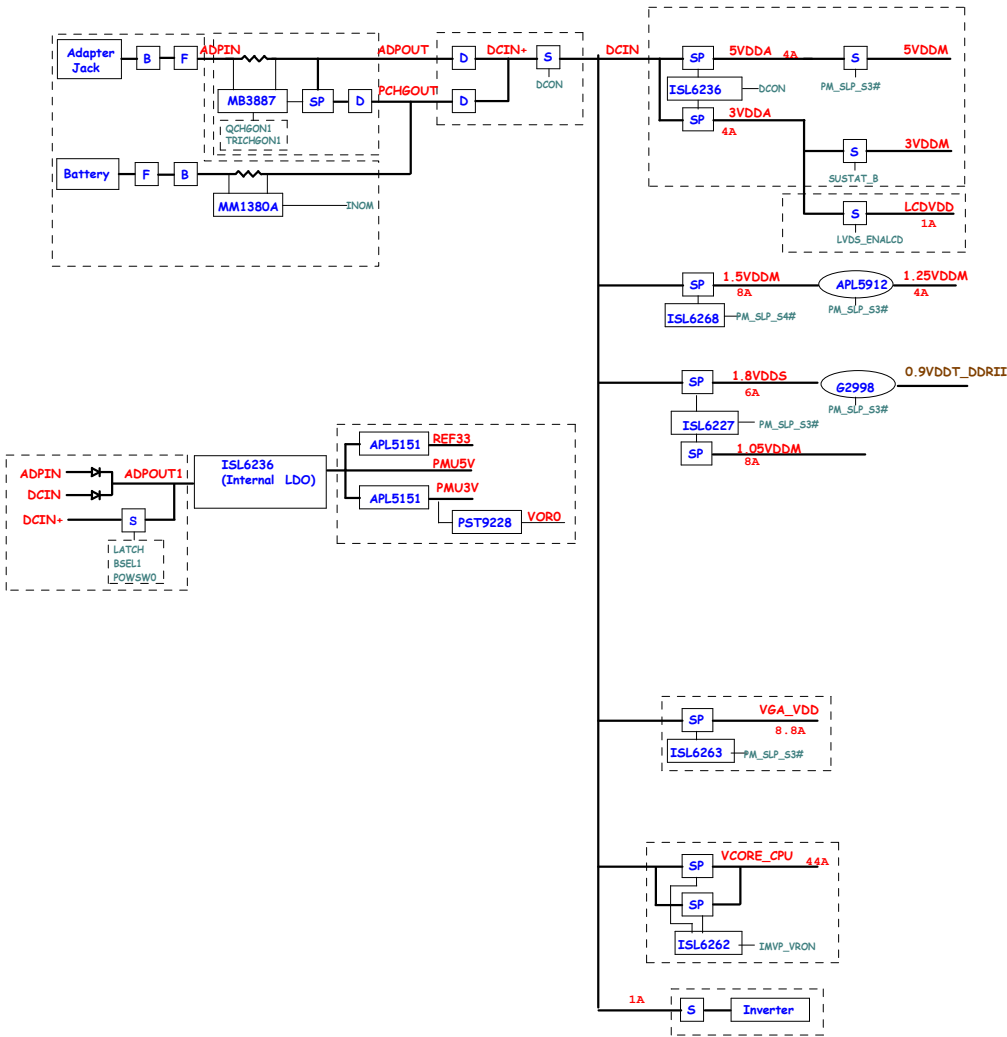
First International Computer, Inc.			
2FL 3RD 300, Yang Guang St, Neihu 114 Taipei, TAIWAN, ROC (886-2)8751-8751			
Title			
MR056B			
Size			
C			
Document Number			
<OVP CKT>			
Rev			
0.1			
Date: Wednesday, June 24, 2008			
Sheet 41 of 53			

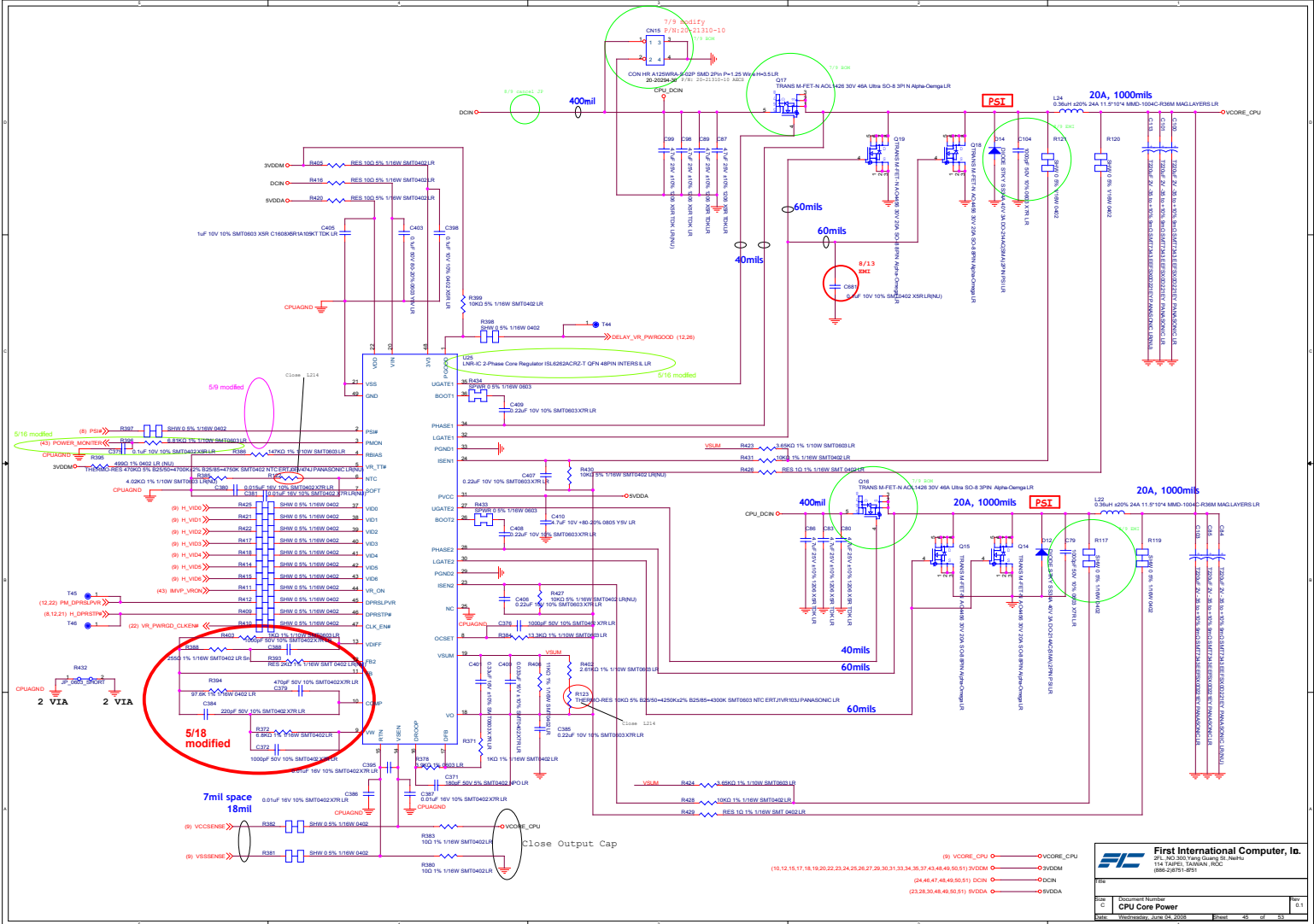
# EMI Solution

C682 : VGA_VDD ---- P.51	C673 : 1.5VDDM ----- P.49
C681 : Q19 pin4 --- P.45	C672 : 1.25VDDM ----- P.49
C680 : R200 pin 1 -- P.46	C671 : 1.5VDDM ----- P.49
C679 : 3VDDA ----- P.48	C670 : 1.5VDDM ----- P.49
C678 : DCIN ----- P.47	C669 : DCIN ----- P.47
C677 : DCIN ----- P.47	C668 : ADPIN ----- P.46
C676 : DCIN ----- P.47	C667 : 1.05VDDM ---- P.50
C675 : DCIN ----- P.47	
C674 : 3VDDA ----- P.48	



## MR055/MR056 Power Block

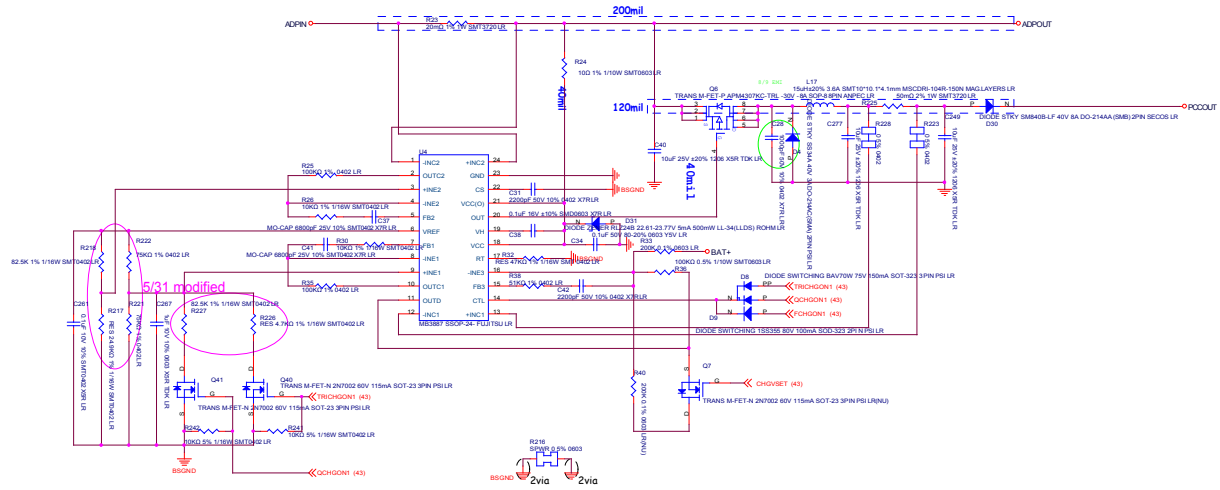




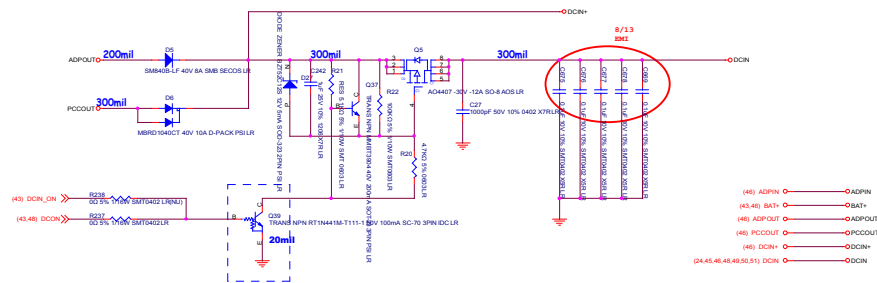
[illegible][illegible]

 <b>First International Computer, Inc.</b> 2FL NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC (886-2)6751-8751	
Title	
<b>MR056B</b> Document Number <b>&lt;AC-IN / Battery CNN&gt;</b>	
Size C	Rev 0.1
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## Charger



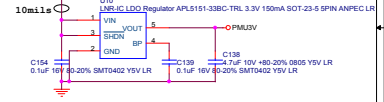
DCIN



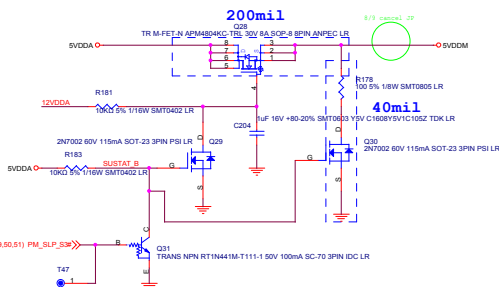
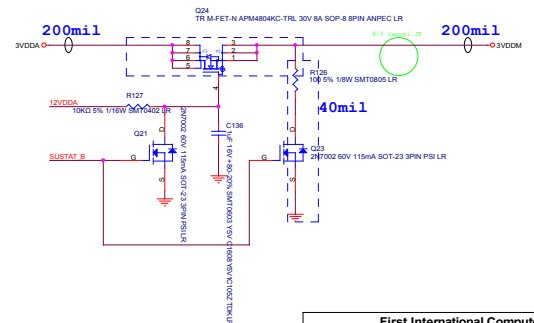
 **First International Computer, Inc.**  
2FL, NO.300, Yang Guang St, Neihu  
114 TAIPEI, TAIWAN, ROC  
(886-2)8751-8751

1250	
------	--

8/9 cancel JP



200mil

Q24  
TR M-FET-N APM

- [illegible]



The image shows a complex PCB layout for a power management system. It includes several key components and annotations:

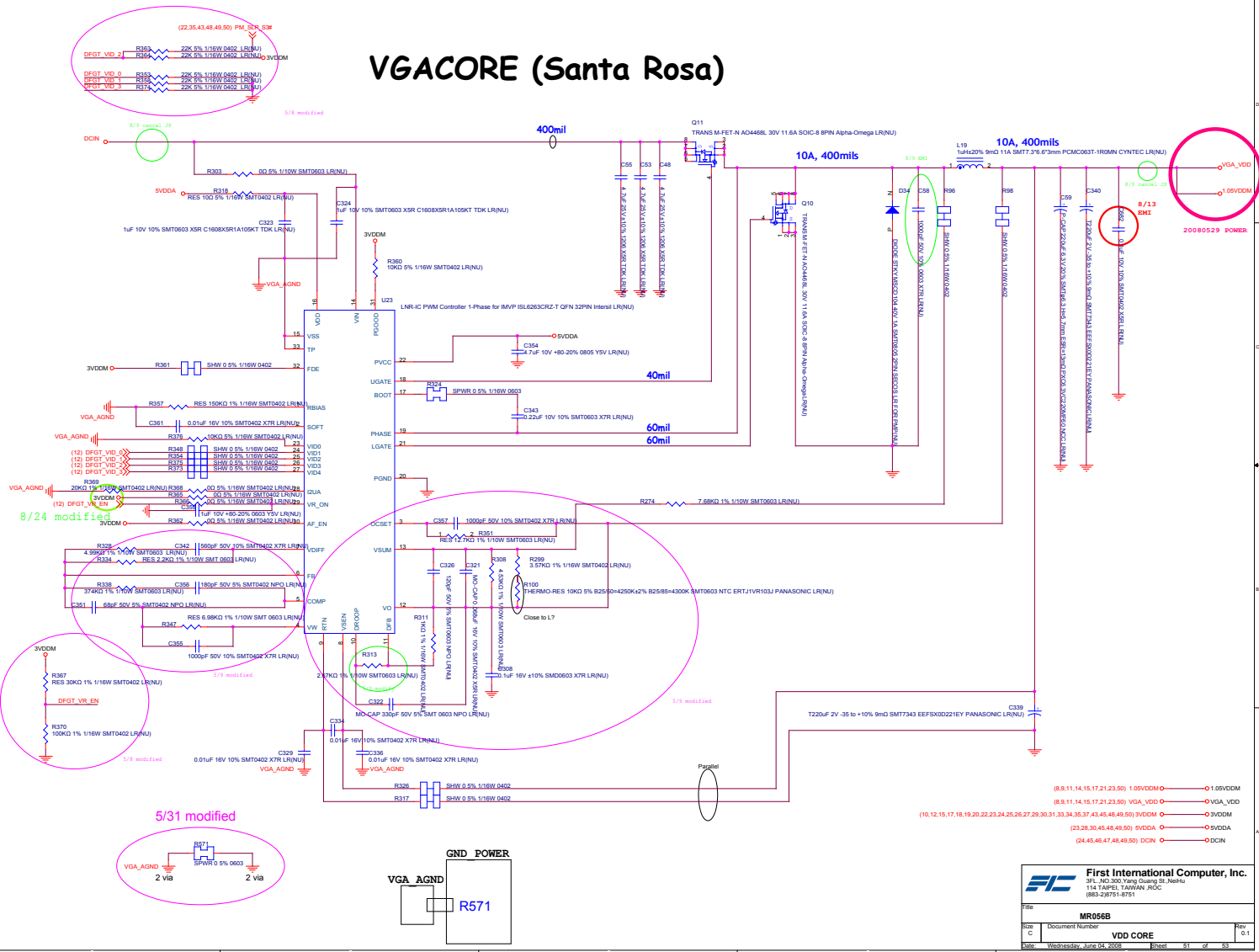
- Power Input:** VIN connected to VDD.
- Grounding:** Multiple GND connections, including a large ground plane labeled "GND".
- Capacitors:** Various electrolytic and ceramic capacitors are placed throughout the board, including C296, C297, C298, C299, C300, C301, C302, C303, C304, C305, C306, C307, C308, C309, C310, C311, C312, C313, C314, C315, C316, C317, C318, C319, C320, C321, C322, C323, C324, C325, C326, C327, C328, C329, C330, C331, C332, C333, C334, C335, C336, C337, C338, C339, C340, C341, C342, C343, C344, C345, C346, C347, C348, C349, C350, C351, C352, C353, C354, C355, C356, C357, C358, C359, C360, C361, C362, C363, C364, C365, C366, C367, C368, C369, C370, C371, C372, C373, C374, C375, C376, C377, C378, C379, C380, C381, C382, C383, C384, C385, C386, C387, C388, C389, C390, C391, C392, C393, C394, C395, C396, C397, C398, C399, C400, C401, C402, C403, C404, C405, C406, C407, C408, C409, C410, C411, C412, C413, C414, C415, C416, C417, C418, C419, C420, C421, C422, C423, C424, C425, C426, C427, C428, C429, C430, C431, C432, C433, C434, C435, C436, C437, C438, C439, C440, C441, C442, C443, C444, C445, C446, C447, C448, C449, C450, C451, C452, C453, C454, C455, C456, C457, C458, C459, C460, C461, C462, C463, C464, C465, C466, C467, C468, C469, C470, C471, C472, C473, C474, C475, C476, C477, C478, C479, C480, C481, C482, C483, C484, C485, C486, C487, C488, C489, C490, C491, C492, C493, C494, C495, C496, C497, C498, C499, C500, C501, C502, C503, C504, C505, C506, C507, C508, C509, C510, C511, C512, C513, C514, C515, C516, C517, C518, C519, C520, C521, C522, C523, C524, C525, C526, C527, C528, C529, C530, C531, C532, C533, C534, C535, C536, C537, C538, C539, C540, C541, C542, C543, C544, C545, C546, C547, C548, C549, C550, C551, C552, C553, C554, C555, C556, C557, C558, C559, C560, C561, C562, C563, C564, C565, C566, C567, C568, C569, C570, C571, C572, C573, C574, C575, C576, C577, C578, C579, C580, C581, C582, C583, C584, C585, C586, C587, C588, C589, C590, C591, C592, C593, C594, C595, C596, C597, C598, C599, C600, C601, C602, C603, C604, C605, C606, C607, C608, C609, C610, C611, C612, C613, C614, C615, C616, C617, C618, C619, C620, C621, C622, C623, C624, C625, C626, C627, C628, C629, C630, C631, C632, C633, C634, C635, C636, C637, C638, C639, C640, C641, C642, C643, C644, C645, C646, C647, C648, C649, C650, C651, C652, C653, C654, C655, C656, C657, C658, C659, C660, C661, C662, C663, C664, C665, C666, C667, C668, C669, C670, C671, C672, C673, C674, C675, C676, C677, C678, C679, C680, C681, C682, C683, C684, C685, C686, C687, C688, C689, C690, C691, C692, C693, C694, C695, C696, C697, C698, C699, C700, C701, C702, C703, C704, C705, C706, C707, C708, C709, C710, C711, C712, C713, C714, C715, C716, C717, C718, C719, C720, C721, C722, C723, C724, C725, C726, C727, C728, C729, C730, C731, C732, C733, C734, C735, C736, C737, C738, C739, C740, C741, C742, C743, C744, C745, C746, C747, C748, C749, C750, C751, C752, C753, C754, C755, C756, C757, C758, C759, C760, C761, C762, C763, C764, C765, C766, C767, C768, C769, C770, C771, C772, C773, C774, C775, C776, C777, C778, C779, C780, C781, C782, C783, C784, C785, C786, C787, C788, C789, C790, C791, C792, C793, C794, C795, C796, C797, C798, C799, C800, C801, C802, C803, C804, C805, C806, C807, C808, C809, C810, C811, C812, C813, C814, C815, C816, C817, C818, C819, C820, C821, C822, C823, C824, C825, C826, C827, C828, C829, C830, C831, C832, C833, C834, C835, C836, C837, C838, C839, C840, C841, C842, C843, C844, C845, C846, C847, C848, C849, C850, C851, C852, C853, C854, C855, C856, C857, C858, C859, C860, C861, C862, C863, C864, C865, C866, C867, C868, C869, C870, C871, C872, C873, C874, C875, C876, C877, C878, C879, C880, C881, C882, C883, C884, C885, C886, C887, C888, C889, C890, C891, C892, C893, C894, C895, C896, C897, C898, C899, C900, C901, C902, C903, C904, C905, C906, C907, C908, C909, C910, C911, C912, C913, C914, C915, C916, C917, C918, C919, C920, C921, C922, C923, C924, C925, C926, C927, C928, C929, C930, C931, C932, C933, C934, C935, C936, C937, C938, C939, C940, C941, C942, C943, C944, C945, C946, C947, C948, C949, C950, C951, C952, C953, C954, C955, C956, C957, C958, C959, C960, C961, C962, C963, C964, C965, C966, C967, C968, C969, C970, C971, C972, C973, C974, C975, C976, C977, C978, C979, C980, C981, C982, C983, C984, C985, C986, C987, C988, C989, C990, C991, C992, C993, C994, C995, C996, C997, C998, C999, C1000.
- Resistors:** Various surface-mount resistors are used for current sensing and voltage division, including R201, R202, R203, R204, R205, R206, R207, R208, R209, R210, R211, R212, R213, R214, R215, R216, R217, R218, R219, R220, R221, R222, R223, R224, R225, R226, R227, R228, R229, R230, R231, R232, R233, R234, R235, R236, R237, R238, R239, R240, R241, R242, R243, R244, R245, R246, R247, R248, R249, R250, R251, R252, R253, R254, R255, R256, R257, R258, R259, R260, R261, R262, R263, R264, R265, R266, R267, R268, R269, R270, R271, R272, R273, R274, R275, R276, R277, R2

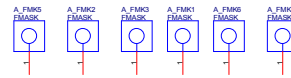
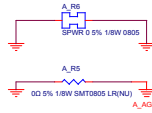
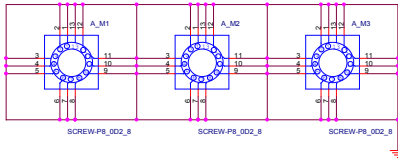
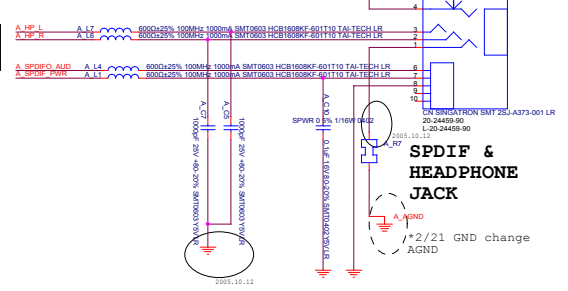
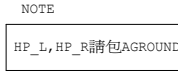
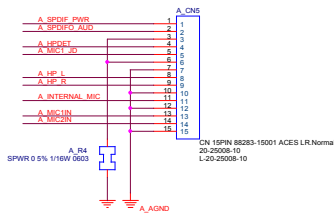
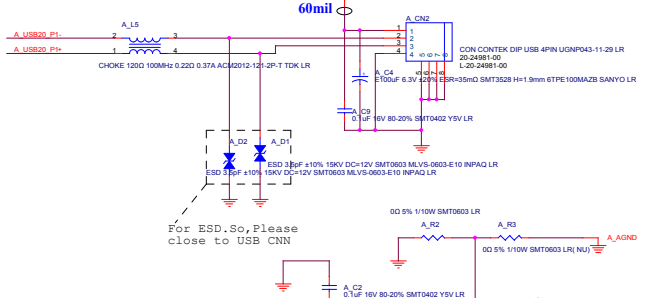
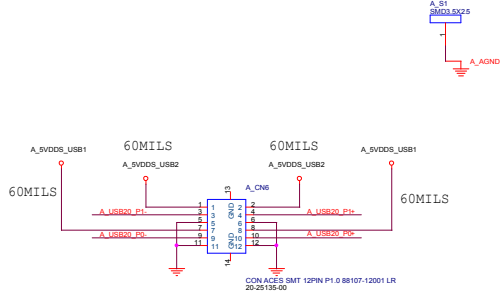
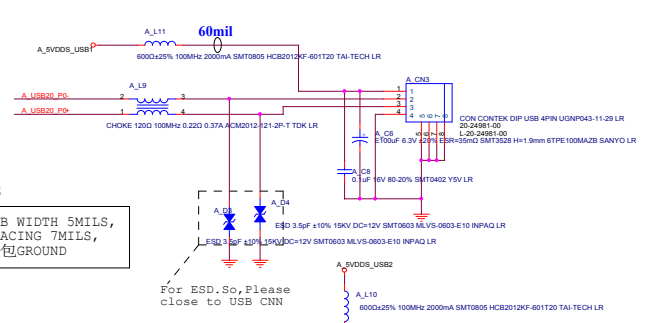
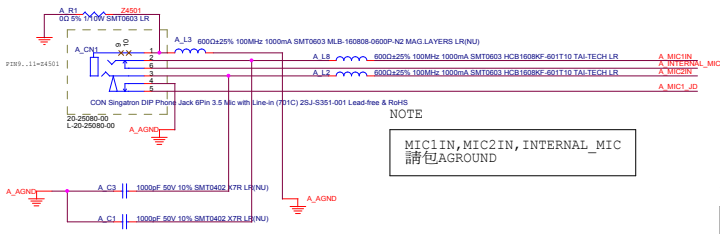
- |   |  |
|---|--|
|  <b>First International Computer, Inc.</b><br>2FL NO.305,Yang Guang St.,Neihu<br>114 TAIPEI, TAIWAN, ROC<br>(886-2)8751-8751 |  |
| Title <b>MR056B</b>   |  |
| Size<br>Country   | Document Number<br><b>1.8VDD5 / 0.9VD DM</b> |
| Date: <b>Wednesday, June 04, 2008</b>   | Rev: <b>0.1</b>                              |
| Sheet <b>49</b> of <b>53</b>  |  |

[illegible]

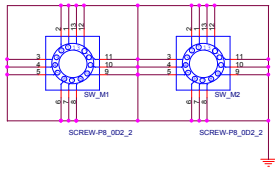
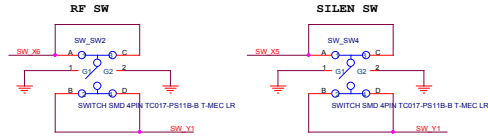
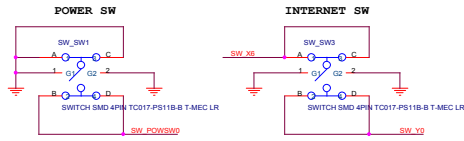
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- (10, 12, 15, 17, 18, 19, 20, 22, 23, 24, 25, 26, 27, 29, 30, 31, 33, 34, 35, 37, 43, 45, 48, 49, 51) 3VDDM
- (8, 9, 11, 14, 15, 17, 21, 23, 51) 1.8VDDM
- (10, 20, 21, 22, 23, 24, 26, 30, 31, 33, 34, 35, 40, 43, 46, 48, 49) 3VDDA
- (23, 28, 30, 45, 48, 49, 51) 5VDDA
- (24, 45, 46, 47, 48, 49, 51) DCIN
- (12, 18, 19) DDR\_VREF
- (18, 19) DDR\_0\_9VDDM
- (12, 14, 15, 18, 19) 1.8VDDOS
- 3VDDM
- 1.8VDDM
- 3VDDA
- 5VDDA
- DCIN
- DDR\_VREF
- DDR\_0\_9VDDM
- 1.8VDDOS

## VGACORE (Santa Rosa)





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Size	Document Number	Rev
C	AUDIO TRANSFER BOARD	0.1
Rev	01	01



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Title: <b>MR056B</b>		
Size: C	Document Number: <b>SWITCH TRANSFER BOARD</b>	Rev: 0.1
Date: Wednesday, June 04, 2008 11:02 AM Page: 53 of 53		